WOCSDICE '95

19'th Workshop on Compound Semiconductor Devices and Integrated Circuits

May 21 - 24, 1995

Stockholm, Sweden

Organised by Ericsson Components AB

Sponsored by Ericsson Components AB
European Research Office, United States Army
ABB HAFO
Geotronics

WOCSDICE '95 PROGRAM SCHEDULE

Monday, May 22

08.30 **Welcome/Opening of workshop**
Jan Söderström

08.40 **Session 1: Materials and Epitaxy**
Chairman: Hartwig Thim

08.45 - 09.10 **Properties and Applications of GaN Films**
Kathleen Doverspike — *Invited*
Naval Research Laboratories — USA

09.10 - 09.20 **Carbon Doping of InGaAs for InP-Based HBTs using Liquid CCl_4 Source**
D. Pavlidis, K. Hong
The University of Michigan — USA

09.20 - 09.30 **GaAs MOVPE Overgrowth of nm-sized Tungsten Wires**
L.E. Wernersson, K. Georgsson, A. Litwin, L. Samuelson, W. Seifert
Lund University — Sweden

09.30 - 09.40 **MOCVD for HBT and HEMT Technology**
F. Schulte, H. Juergensen
Aixtron Semiconductor Technologies GmbH — Germany

09.40 - 09.50 **Limitation in concentration and mobility for Si δ-doping and Si monolayers in GaAs**
J. Thordson, P. Songpongs, *T.G. Andersson*
Chalmers University of Technology — Sweden

09.50 - 10.00 **Modification of InGaAs/InAlAs Hetero-Barriers by Delta Doping**
D.W.E. Allsopp, M. Cerniansky, M. Hopkinson
University of York — U.K.

10.00 - 10.10 **New Electronic Materials: Low Temperature Grown GaAs and InP**
W.M. Chen, E. Sörman, B. Monemar, P. Dreszer, A. Prasad, X. Liu, E.R. Weber, B.W. Liang, C.W. Tu
Linköping University — Sweden

10.10 - 10.40 Coffee break

WOCSDICE '95 PROGRAM SCHEDULE

Monday, May 22

10.40 **Session 2: Optoelectronic Devices I**
Chairman: Lester F. Eastman

10.45 - 11.10 **Semiconductor Laser Reliability**
Mitsuo Fukuda — *Invited*
NTT Opto-electronics laboratories — Japan

11.10 - 11.20 **Reliability of MOCVD Grown AlGaInP Surface Emitting LEDs**
D.V. Morgan, *Y.H. Aliyu*, H. Thomas
University of Wales College Cardiff — U.K.

11.20 - 11.30 **Photoluminescence Study of Carrier Transport in InGaAsP Quantum Well Laser Structures**
S. Marcinkevicius, *U. Olin*, C. Silfvenius, B. Stålnacke, J. Wallin, G. Landgren
Royal Institute of Technology — Sweden

11.30 - 11.40 **Temperature effects of the performance of high speed quantum well lasers**
Robert M. Spencer, S. S. O'Keefe, C. Yi Tsai, J. Greenberg, J. Braunstein, G.H. Martin, W.J.Schaff, L.F. Eastman
Cornell University — USA

11.40 - 11.50 **4 x 4 Switch Design and Characterization**
Wilhelmus van Berlo
Ericsson Components AB — Sweden

11.50 - 12.00 **Optoelectronic Integrated Circuits Based on Commercially Processed GaAs IC's**
Clifton G. Fonstad
Massachusetts Institute of Technology — USA

12.00 - 12.10 **Fabrication of and Photoluminescence from InGaAsP Microdiscs**
B. Corbett, J. Justice, L. Considine, S. Walsh, W.M. Kelly
University College Cork — Ireland

12.10 - 12.20 **Confinement effect on excitons in self-organized InGaAs quantum disks**
H. Weman, H. Kamada, M. Potemski, J. Temmyo, R. Nötzel, T. Tamamura
Linköping University — Sweden

12.20 - 12.30 Room for late paper

12.30 - 14.00 Lunch

WOCSDICE '95 PROGRAM SCHEDULE

Monday, May 22

14.00 **Session 3: Optoelectronic Devices II**
Chairman: Theo van de Roer

14.05 - 14.30 **Long wavelength vertical cavity surface emitting lasers**
Anders Karlsson *Invited*
Royal Institute of Technology Sweden

14.30 - 14.40 **Vertical Cavity Surface Emitting Laser Characterization by Photoreflectance Spectroscopy**
P.D. Berger, C. Bru, T. Benyattou, G. Guillot, A. Chenavas-Paule, P. Grosse
Laboratoire de Physique de la Matière France

14.40 - 14.50 **Heavily C-doped GaAs/AlGaAs Multi-Quantum-Well Normal Incidence Infrared Photodetectors**
E. Mao, B.W. Kim, A.H. Lu, S.A. Dickey, *A. Majerfeld*,
University of Colorado USA

14.50 - 15.00 **Effect of Substrate Misorientation on the Electrical and Optical Properties of AlGaInP LEDs**
D.V. Morgan, *Y.H. Aliyu*, H. Thomas, D. Lacey
University of Wales College of Cardiff U.K.

15.00 - 15.10 **Resonant cavity enhanced InGaAs/AlGaAs Heterojunction**
O. Sjölund, A. Larsson
Chalmers University of Technology Sweden

15.10 - 15.20 **Novel InP/GaInAs Photodetector for a Simple Integration in HEMT Circuits**
M. Horstmann, M. Marso, F Rüders, M. Hollfelder, P. Kordos, H. Lüth
Forschungszentrum Jülich Gmbh Germany

15.20 - 15.30 **New type of Photodetectors - Injection Photodiodes based on Graded III-V semiconductors**
H.P. Peka, V. Radziviliuk, A.V. Buyanov
Kiev University Ukraine

15.30 - 15.40 Room for late paper

15.40 - 16.10 Coffee Break

WOCSDICE '95 PROGRAM SCHEDULE

Monday, May 22

16.10 **Session 4: Novel Structures and Concepts**
Chairman: Erhard Kohn

16.15 - 16.40 **Potentials of SiGe Heterobipolar and Heterofieldeffect Transistors**
Andreas Gruhle, U. König — *Invited*
Daimler Benz Research Center — Germany

16.40 - 16.50 **Novel Superlattice Limiter Diodes**
D.G. Hayes, A.W. Higgs, D.D. Besgrove, D.C. Herbert, P.J. Wilding, G.W. Smith, K.P. Hilton
DRA Malvern — U.K.

16.50 - 17.00 **Exciton Lifetimes in GaN and GaInN**
C.I. Harris, J.P. Bergman, *B. Monemar*, H. Amano, I. Akasaki
Linköping University — Sweden

17.00 - 17.10 **Enhanced Mobility Piezoelectric HEMT Structures on (111)B InP Substrates**
L.J. Hitchens, *P.A. Houston*, M. Hopkinson, G.J. Rees
The University of Sheffield — U.K.

17.10 - 17.20 **A Millimeter-Wave Interferometer for Measurements of small displacements using a FECTED-VCO**
A. Stelzer, A.L. Springer, C.G. Diskus, K. Lübke, *H.W. Thim*
The University of Linz — Austria

17.20 - 17.30 **Preparation and Characterisation of Quantum Dots of ZnSe/CdZnSe/ZnSe grown by MBE on GaAs**
T.G. Andersson, M. Illing, T. Kümmel, G. Bacher, A. Forchel, D. Hommel, B. Jobst, G. Landwehr
Chalmers University of Technology — Sweden

17.30 - 17.40 **InAs/$Ga_{1-x}In_xSb$ Superlattices for Long-Wavelength Applications Grown on GaAs Substrates**
J.H. Roslund, G. Swensson, T.G. Andersson
Chalmers University of Technology — Sweden

17.40 - 17.50 **Improving the Schottky Barrier and Leakage Current of MODFETs grown on InP**
M. Seaford, G. Martin, S. Massie, D. Hartzell, L.F. Eastman
Cornell University — USA

17.50 - 18.00 Room for late paper

WOCSDICE '95 PROGRAM SCHEDULE

Tuesday, May 23

08.00 **Session 5: Modeling / Simulation**
Chairman: Hans Hartnagel

08.05 - 08.30 **Simulation Methods for Submicron Compound Semiconductor Devices**
Kazutaka Tomizawa — *Invited*
Meiji University — Japan

08.30 - 08.40 **A Physical Description of the Behavior of GaAs MESFETs in the Deep Linear Region**
R. Menozzi, M. Bertoldi, F. Fantini, G. Green
The University of Parma — Italy

08.40 - 08.50 **Large-Signal Design Considerations of InP/InGaAs Heterojunction Bipolar Transistor-based OEICs**
D. Pavlidis, A. Samelis, S. Chandrasekhar, L.M. Lunardi
The University of Michigan — USA

08.50 - 09.00 **Design Considerations for Low-Noise Applications of SiGe HBTs**
U. Erben, H. Schumacher
University of Ulm — Germany

09.00 - 09.10 **On the Influence of the Interface States of HBTs**
J. Grajal, V. Krozer, H.L. Hartnagel, J. Gismero
Polytechnical University of Madrid — Spain

09.10 - 09.20 **AlGaN/GaN MODFET Performance**
L.F. Eastman, J. Burm, W.J. Schaff
Cornell University — USA

09.20 - 09.30 **Capacitance Model for Double Barrier Resonant Tunneling Diodes**
T.G. van de Roer, H.C. Heyker, M. Kwaspen, M. Lepsa, W. van der Vleuten
Eindhoven University of Technology — The Netherlands

09.30 - 09.40 **New MODFET Equivalent Circuit Model: Extraction and Validation to 120 GHz.**
P.J. Tasker
Fraunhofer Institut für Angewandte Festkörperphysik (IAF) — Germany

09.40 - 10.10 Coffee break

WOCSDICE '95 PROGRAM SCHEDULE

Tuesday, May 23

10.10 **Session 6: Transistors I**
Chairman: Fausto Fantini

10.15 - 10.40 **Microwave HBT Power Devices and Applications**
Burhan Bayraktaroglu *Invited*
Westinghouse Electric USA

10.40 - 10.50 **MOVPE growth and characterization of carbon-doped $In_{0.47}Ga_{0.53}As/InP$ HBT**
A Wiersch, A. Lindner, Q. Liu, F. Scheffer, D. Peters, W. Prost, E. Kuphal, *F.J. Tegude*
Gerhard-Mercator University Duisburg Germany

10.50 - 11.00 **GaAlAs/GaAs and GaInP/GaAs HBT's for Power Applications**
J.P. Bailbé, J. Tasselli, L. Andrieux, H. Granier, T. Camps, A. Cazarré, A. Marty, M. Faleh
Laboratoire d'Analyse et d'Architecture des Systèmes du CNRS France

11.00 - 11.10 **Hole Barrier Bipolar Transistors using InGaP/GaAs**
C.Saavedra-Munoz, D.W. Woodard, K. Whittingham, L.F. Eastman, L.W. Yang
Cornell University USA

11.10 - 11.20 **Hot Electron Noise in an AlGaAs-Based Triple-Heterojunction Channel**
A. Matulionis, V. Aninkevicius, V. Bareikis, J. Liberis, I. Matulioniené, P.S. Kop'ev, V.M. Ustinov
Semiconductor Physics Institute Lithuania

11.20 - 11.30 **Noise in Channel Doped GaInP/InGaAs-HFET-Devices**
D. Geiger, E. Mittermeier, J. Dickmann, C. Geng, R. Winterhoff, F. Scholz, E. Kohn
University of Ulm Germany

11.30 - 11.40 **Isothermal Electric Breakdown in MESFET and MODFET**
Ya.B. Martynov, *A.S. Tager*
SR & PC 'ISTOK' Russia

11.40 - 13.10 Lunch

WOCSDICE '95 PROGRAM SCHEDULE

Tuesday, May 23

13.10 **Session 7: Processing**
Chairman: Vernon Morgan

13.10 - 13.20 **Dry etched Fabry-Perot (FP)-{110} facets of 1.55 μm (RW)-laser**
K. Vogel, J. Würfl
Ferdinand-Braun-Institut für Höchstfrequenztechnik Berlin Germany

13.20 - 13.30 **Enhanced Chemically-Assisted Ion-Beam Etching Process for High-Speed GaAs-Based MQW Lasers**
R.E. Sah, J.D. Ralston, K. Eisele, S. Weisser, W. Benz
Fraunhofer Institut für Angewandte Festkörperphysik (IAF) Germany

13.30 - 13.40 **The Influence of $CH_4/H_2/Ar$ ECR Plasma Etching on GaAs-Based Heterostructures for Field Effect Transistors**
J.G. van Hassel, C.M. van Es, P.A.M. Nouwens, L.M.F. Kaufmann
Eindhoven University of Technology The Netherlands

13.40 - 13.50 **Investigation of CH_4/H_2/ RIE for Gate Recess Etching in InGaAs/InAlAs-based HEMTs**
H.C. Duran, W. Patrick
Swiss Federal Institute of Technology Zürich Switzerland

13.50 - 14.00 **High Barrier Schottky Contacts on n-InP using Damage Free Electrochemical Metallization**
D.C. Dumka, R. Riemenschneider, J. Miao, H.L. Hartnagel B.R. Singh
Institut für Höchstfrequenztechnik, Darmstadt Germany

14.00 - 14.10 **Ohmic Contact Degradation in AlGaAs/GaAs HEMTs**
W.T. Anderson, K.A. Christianson, C. Moglestue
Naval Research Laboratory, Washington USA

14.10 - 14.20 **Comparison of AuGe/Ni ohmic-and Ti Schottky-Contact on n^+-GaAs for RF-Power Generation above 140 GHz**
J. Freyer, M. Tschemitz
Technical University of Munich Germany

14.20 - 14.30 **Metallizations for GaAs MMICs operating at elevated temperatures up to 300 °C**
J. Würfl, E. Nebauer, *U. Merkel*, K. Vogel
Ferdinand.Braun-Institut für Höchstfrequenztechnik Berlin Germany

14.30 - 15.00 Coffee and walk to tour boats

15.00 - 17.00 Sightseeing: Stockholm seen from the water

17.00 - 18.00 Tour of Royal Castle

18.00 - 23.00 Workshop dinner at M/S Waxholm III

WOCSDICE '95 PROGRAM SCHEDULE

Wednesday, May 24

08.30 **Session 8: Transistors II**
Chairman: Dimitris Pavlidis

08.35 - 09.00 **GaAs-MMIC Applications in Wireless and Fiber Optic Telecommunication Systems**
Mikael Snellman *Invited*
Ericsson Components AB Sweden

09.00 - 09.10 **GaInP/GaAs HBT MMIC Power Amplifiers at X-Band**
H. Blanck, S.L. Delage, D. Floriot, S. Cassette, E. Chartier, M-A. di Forte-Poisson, D. Pons, P. Roux, E. Watrin, P. Chaumas, P. Bourne
Thomson CSF France

09.10 - 09.20 **Advanced PMHFET GaAs MMIC Components for Ka-Band Communication Systems**
P. Narozny, H. Dämbkes, J.M. Dieudonné, B. Adelseck
Daimler Benz Research Center Germany

09.20 - 09.30 **Compact High Gain Low Noise 60 to 80 GHz Amplifiers on GaAs**
J. Braunstein, P.-J. Tasker, M. Schlechtweg, H. Massler, A. Hülsmann, K. Köhler, W. Bronner, Jo. Schneider
Cornell University USA

09.30 - 09.40 **Monolithic Demodulator for High-Sensitivity 5 Gbit/s CPFSK Receiver using a Distributed Mixing Principle**
P. Karlsen, F. Ebskamp, A.K. Petersen, *P. Danielsen*
Technical University of Denmark Denmark

09.40 - 09.50 **High Performance Circuits using AlInAs/GaInAs/InP HEMTs**
W. Patrick, M. Schefer, B-U.H. Klepser, H.C. Duran, Hp. Meier
Swiss Federal Institute of Technology Switzerland

09.50 - 10.00 **Transconductance Dispersion in LT GaAs MISFET's**
B. Boudart, E. Delos, F. Ducroquet, H. Gérard, D, Théron, M. Lipka, B. Splingart, E. Kohn
Institut d'Electronique et de Microél. du Nord France

10.00 - 10.10 **Delay Times in Lattice Matched InGaAs/InP HEMT's with Gatelengths between 80 and 250 nm**
J. Finders, Y. Baeyens, D. Schreurs, M. Van Hove, W. De Raedt, B. Nauwelaers, M. Van Rossum
IMEC Interuniversity Microelectronics Center Belgium

10.10 - 10.40 Coffee break

WOCSDICE '95 PROGRAM SCHEDULE

Wednesday, May 24

10.40 **Session 9: Characterization**
Chairman: Paul Tasker

10.45 - 11.10	**On-Wafer Electro-Optic Testing of High-Speed Electronic Devices** *Mike Jackson* University of British Columbia	*Invited* Canada
11.10 - 11.20	**Fourier Transform Photoluminescence Excitation Spectroscopy of InGaAs/InP Quantum Wells with various strain and well width** *J. Dalfors*, T. Lundström, P.O. Holtz, B. Monemar, J. Wallin, G. Landgren Linköping University	Sweden
11.20 - 11.30	**Photoconduction and Internal Photoemission in PHEMTs** *F. Schuermeyer*, C. Cerny, R. Dettmer, J.P. Loehr, R.E. Sherriff Wright Patterson AFB, Ohio	USA
11.30 - 11.40	**Characterization of p-type modulation-doped SiGe Heterostructures by Optical Spectroscopies** *I.A. Buyanova*, W.M. Chen, A. Henry, W.X. Ni, G.V. Hansson, B. Monemar Linköping University	Sweden
11.40 - 11.50	**Electron Transport through GaAlAs Barriers** *J.C. Bourgoin* Universités Paris 6 et 7	France
11.50 - 12.00	**Luminescence and Magnetotransport Studies of InP-based HEMT structures** *W.E. Leitch*, B. Henle, E. Kohn University of Ulm	Germany
12.00 - 12.15	Workshop conclusion	
12.15 - 13.00	Lunch and check-out	
13.10	Bus to Ericsson Components AB	
13.45 - 15.15	Tour of Ericsson submicron processing facility	
15.15	Bus from Ericsson Components to Arlanda airport	
16.00	Arrival at Arlanda airport	

MONDAY

SESSION 1

MATERIALS AND EPITAXY

"Properties and Applications of GaN Films",

Kathy Doverspike
Naval Research Laboratory, Code 6861
Washington, DC 20375-5000 USA

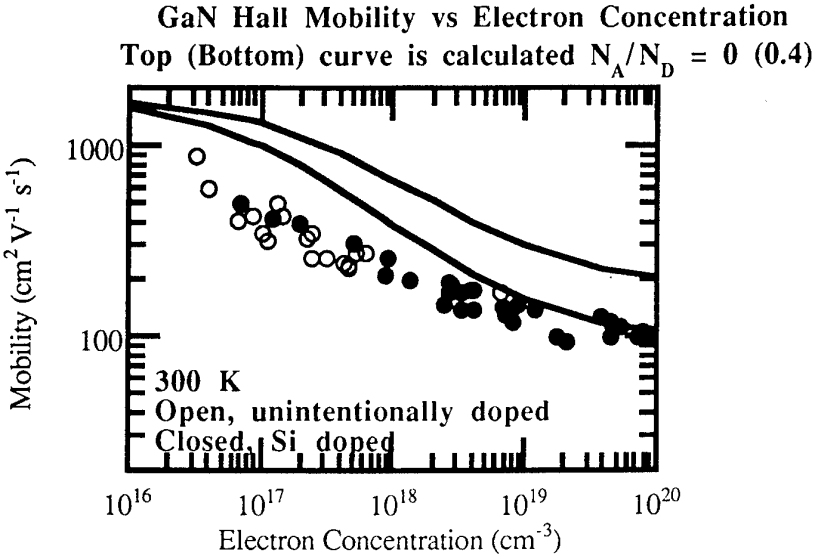
LEDs are an important class of devices which can convert electricity to light very efficiently. For many applications including full color displays, bright green and blue LEDs are essential in addition to the bright red already available. Although blue LEDs based on SiC have been commercially available for approximately 10 years, the efficiency is low due to the indirect bandgap of SiC. GaN and its alloys with InN and AlN provide a class of compounds which have large bandgaps making them suitable, not only for blue and blue-green LEDs, but also for UV emitters, detectors and high frequency, high temperature FET devices. There has been a recent surge of interest in GaN, in part because of improvements in the materials growth of GaN. Low temperature buffer layers are now commonly used to reduce the large lattice mismatch between GaN and sapphire. The improvement in the material quality has also led to decreasing the background carrier concentration for a given GaN layer thickness. Many researchers can currently obtain a background concentration in the mid 10^{16} cm^{-3} range for thin films a few microns thick, whereas in the 1970's GaN with a similar carrier concentration grown by halide vapor phase epitaxy had to be >100μm. This decrease in the background carrier concentration has enabled researchers to dope the material both n- and p-type. Blue and blue-green LED's are now commercially available from Nichia in which a InGaN-AlGaN double heterostructure structure is used.

Most of the GaN growth to date has used sapphire as the substrate, although other substrates are being investigated which include SiC, MgO, ZnO, Si, and GaAs. The lack of a lattice-matched substrate has made the epitaxial growth of GaN very challenging. It has been shown that the deposition conditions of the buffer layer (temperature and thickness) has a drastic effect on the resulting quality of the GaN films. Other growth parameters that have been studied that show a significant effect on the quality of GaN are sapphire substrate orientation, V/III ratio, and growth temperature.

The figure on the following page shows the best reported Hall mobility versus carrier concentration for GaN as reported by various groups. The solid lines shown on the figure are the results of theoretical modeling assuming different amounts of compensation. This data is for both types of buffer layers (GaN and AlN) and for both OMCVD and MBE grown films, although the majority of the points are for films grown by OMCVD. It is interesting to note that in the areas where there is overlap between the

unintentionally doped films and the Si-doped films, the data follows the same trend. This implies that the magnitude of compensation in these films is approximately the same.

The defect density in GaN layers on sapphire are relatively high (commonly $10^{10}/cm^2$ defects are observed). The main defects observed are primarily threading dislocations that we believe may be formed at low angle grain boundaries during the initial stages of GaN growth (during which coalescence of islands takes place). In this system, since the dislocations run along the [0001] growth direction, we do not observe a decrease in dislocation density with GaN film thickness. Currently, strained layered superstructures are being investigated as a mechanism to decrease the dislocation density.



To fabricate high frequency FET devices using GaN, one not only needs the ability to grow high mobility GaN, but also semi-insulating GaN in order to separate the active channel layer from any low mobility conduction pathways in the defective region near the GaN/sapphire interface. Comparing the properties of the doped GaN films on sapphire also gives us an indication of the quality of the undoped semi-insulating GaN (i.e. higher mobility doped GaN indicates higher quality semi-insulating GaN). Photoluminescence spectroscopy done at 6K has also revealed free exiton emission in the undoped semi-insulating material implying that high quality GaN with a much lower background carrier concentration can be achieved. The photoluminescence spectra of Si-doped GaN shows an enhanced emission with a 25meV shift from the bandedge. This is in agreement with the silicon donor ionization energy of 26meV which is obtained from variable temperature Hall measurements.

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Carbon Doping of InGaAs for InP-Based HBTs Using Liquid CCl_4 Source

D. Pavlidis and K. Hong
Department of Electrical Engineering and Computer Science,
The University of Michigan, Ann Arbor, MI 48109-2122, USA

Heavily doped p-type InGaAs is of crucial importance for high performance Heterojunction Bipolar Transistors (HBTs) since it allows resistance reduction of the relatively thin base and thus better high-speed operation. The use of carbon as base dopant offers an alternative to traditionally used dopants such as Be and Zn since it is known that it offers the possibility of lower atomic diffusion coefficient in materials such as GaAs. C-doping in InGaAs may consequently avoid base dopant redistribution which causes performance degradation and poor reliability in HBTs. Most of the work on C-doping of InGaAs has been with MBE-based approaches. A few reports have also been made using gaseous CCl_4 in MOCVD. Liquid rather than gaseous CCl_4 offers easier installation and a wider range of dopant flux as necessary for optoelectronic applications; the bubbler temperature and pressure can also be used as control parameters in this case. This paper reports on the use of liquid CCl_4 for carbon doping of InGaAs and the mechanisms affecting the effective doping level. The base contact resistance advantage offered by heavily C-doped InGaAs is also discussed.

The layers were grown in our EMCORE LP-MOCVD system using TMIn, TMGa for group III and 100% AsH_3 for group V elements. C-InGaAs imposes an additional difficulty compared with C-GaAs due to the amphoteric character of carbon. Growth conditions were therefore optimized so that carbon is primarily incorporated in As rather than group III sites and p-type material could be obtained. Low growth temperature (<500°C) and V/III ratios (~5) were used for this purpose. Both the TMGa and TMIn incorporation efficiency were found to be reduced in the range of 430°C to 550°C when CCl_4 was present. This is in contrast to gaseous CCl_4 where only the In incorporation is affected. However, the reduced Ga incorporation is found to be relatively insensitive to growth temperature (T_{gr}), unlike the In efficiency which reduced with T_{gr}. It appears therefore that reduced T_{gr} allows one to minimize growth rate reduction due to the presence of CCl_4. Moreover, our studies demonstrate that this choice allows alloy compositions which are insensitive to the amount of CCl_4.

The possibility of hydrogen incorporation in the C-doped samples of our study has been investigated by performing isothermal and isochronal annealing experiments. Hydrogen is known to result in reversible passivation of donors and acceptors in III-Vs and can thus limit the degree of effective doping. Samples grown at 430°C showed after post-growth annealing at 600°C a maximum hole concentration of $6.5 \times 10^{19} cm^{-3}$ which corresponds to an order of magnitude increase compared with the as grown hole concentration (Fig.1). The mobility is also found to increase after annealing. SIMS analysis (Fig.2) revealed depassivation after annealing. However, the doping increased much more than the depassivated atoms. By employing SIMS and Hall data we show in Fig.3 that the ratio of hydrogen to carbon passivated atoms decreases from 63% to 14% while carbon is displaced from group III to group V sites. Thus a combined effect of hydrogen depassivation and carbon displacement appears to take place upon annealing.

The possibility of employing the C-doped InGaAs layers in the external base of InP-based HBTs was investigated. Structures consisting of a 5000Å thick InGaAs subcollector ($n\sim 2 \times 10^{19} cm^{-3}$), 4000Å InGaAs collector ($n\sim 1 \times 10^{17} cm^{-3}$), a Zn-doped InGaAs base ($p\sim 8 \times 10^{18} c m^{-3}$) and a carbon doped InGaAs layer on top were investigated for this purpose. The results shown in Fig.4 demonstrate that the specific contact resistance can be reduced from $4x10^{-5} ohm\text{-}cm^2$ to $5x10^{-7} ohm\text{-}cm^2$ by employing C-doped annealed InGaAs.

Overall, the use of liquid CCl_4 for carbon doping of InGaAs is reported and the mechanisms of its incorporation are studied revealing combined hydrogen passivation and carbon displacement upon annealing. The developed technology can be very useful in applications such as the realization of HBTs with low base resistance.

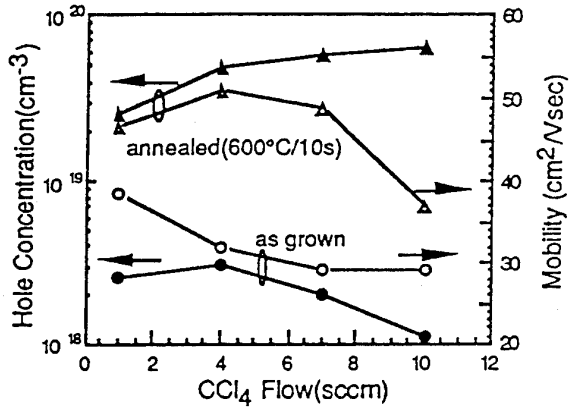

Fig.1 Impact of annealing on the hole concentration and mobility of C-InGaAs

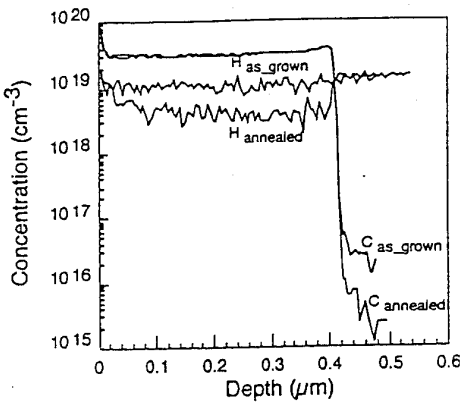

Fig.2 SIMS analysis of C-InGaAs before and after annealing

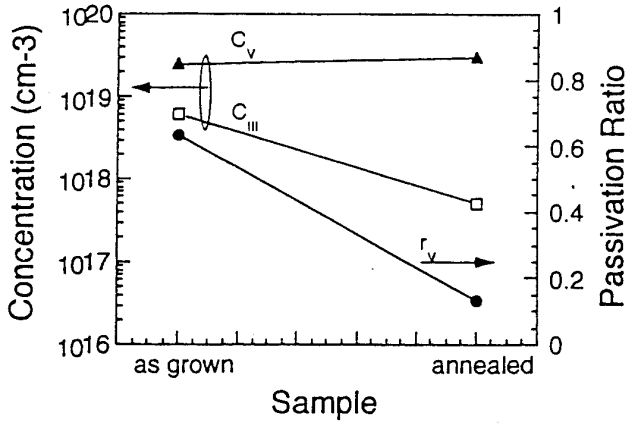

Fig.3 C-occupation of group III and V sites (C_{III} and C_V) and H-passivation ratio r_V before and after annealing

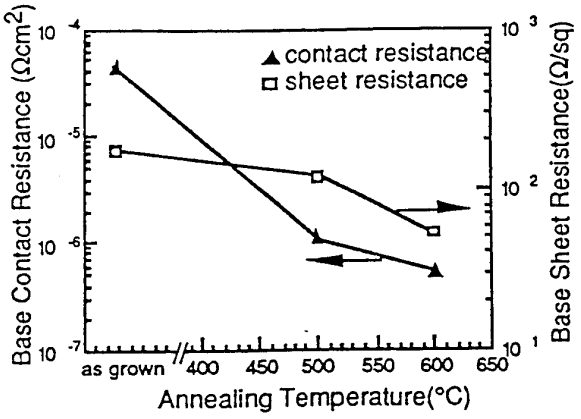

Fig. 4 Impact of C-InGaAs annealing on contact resistivity and base sheet resistance

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Work supported by ARPA-COST (MDA 972-94-1-0004) and ARO (DAAL 03-92-G-0109)

GaAs MOVPE Overgrowth of nm-Sized Tungsten Wires

LE Wernersson, K Georgsson, A Litwin*, L Samuelson, W Seifert

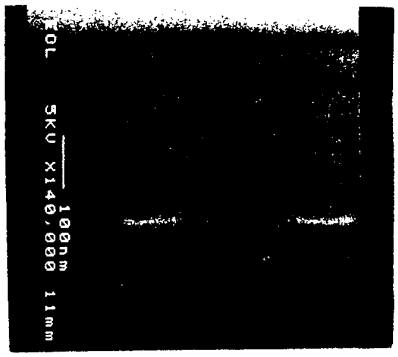
Dept. of Solid State Physics/Nanometer "Structure" Consortium Lund University, Sweden

*also at Ericsson Components AB Kista-Stockholm, Sweden

In the past, attempts have been made to realize the Permeable Base Transistor (PBT) by overgrowing W structures with GaAs. The PBT is expected to have an advantage in its high frequency response and an extrapolated fmax of 265 GHz has been published. Ballistic transport is proposed to play an important role in the electron transport, due to the extremely thin base layer. A transistor structure with a emitter to collector length comparable to the ballistic transport lenght in GaAs, is an interesting tool for studying the transport properties on this length scale.

We report on epitaxial overgrowth by Metalorganic Vapour Phase Epitaxy (MOVPE) of nm-sized tungsten (W) structures on GaAs. Our goals are to investigate and visualize the planarization of the overgrowth as a function of the grating angle and grating period on the nanometer length scale. Further, the electrical properties of the overgrown contacts are investigated.

We used electron beam lithography, evaporation of metal and conventional lift-off technique to produce W patterns on GaAs substrates. The samples were cleaned and transferred to a MOVPE reactor, where the overgrowth was done at a temperature of 630 C and at a pressure of 50 mbar. Inspections of the structures were performed with a high resolution field emission scanning electron microscope (FE-SEM), both on top surface and on cleaved surfaces. We found that is is possible to obtain a completely planarized growth front after 200 nm of growth, when the metal is no wider than 100 nm. Finally, the electrical properties were characterized by I-V measurements of Schottky diodes formed between the grid and the overgrown material. A low reverse current is observed, indicating good electrical properties of the material and the interfaces.



SEM image of AlAs marker layers introduced in the GaAs overgrowth of W

MOCVD for HBT and HEMT Technology

F. Schulte, H. Juergensen

AIXTRON Semiconductor Technologies GmbH, Kackertstraße 15–17,
52072 Aachen, Germany, Tel: +49 (241) 8909–0, Fax: +49 (241) 8909–40

ABSTRACT

For HBT's and HEMT's the MOCVD is a suitable technology for production of uniform, high quality layers and structures. Today commercially available discrete devices and amplifier units, respectively, based on the GaAlAs/Ga(In)As material system are on the market. The tendency is to move toward Al– free material systems since fabrication technology is simpler and the device characteristic is improved. Excellent phosphorous containing material like GaInP/GaAs heterostructures for fabrication of HBT or HEMTs have been grown by MOCVD. The Planetary Reactor™ MOCVD guarantees reproducible multiwafer production of 2", 3" and 4" wafers. Together with the advantage of low defect levels on the wafer the Planetary Reactor™ MOCVD is a proven, cost efficient fabrication tool commercially available on the market and offering multiwafer production for both GaAs and InP technology.

In this paper we will report on results on control of heterostructure, Quantum Well growth and uniformity across large areas (2", 3", 4" wafers) all of which are requested for device technology. Thickness uniformity on a single wafer of better than 0.2% and from wafer to wafer in one run less than 0.8% will be presented. The sheet resistance uniformity on a 4" wafer is < 0.43%. On a 2" wafer the variation of sheet carrier concentration of the 2– dimensional electron gas is within +/– 1%. The threshold voltage uniformity of HEMT devices is +/– 33mV. Very high doping levels to reduce the base resistance as requested in HBT technology have been achieved: With Carbon doping using TMAs as precursor material up to 1 x 10^{20} cm^{-3} has been achieved.

DC– and RF results of HEMT and HBT devices and circuit will be shown. The characteristics will also be discussed under the aspects of reproduciblity from run to run and from wafer to wafer.

Limitation in concentration and mobility for Si δ-doping and Si monolayers in GaAs

J Thordson, P Songpongs[†] and T G Andersson

Department of Physics, Chalmers University of Technology and Göteborg University

S-412 96 Göteborg, Sweden.

In this work we have studied the free carrier concentration and mobility in GaAs as a function of temperature for a wide Si δ-doping range; $5 \cdot 10^{11}$ - $9 \cdot 10^{13}$ cm^{-2}, and the growth of atomic planes; 0.1 - 6 MLs, to study the useful range of carriers and the GaAs/Si/GaAs heterostructure formation for a Si-plane that is positioned 0.1 μm from the surface. The growth temperature, ~ 500 °C, was low enough to minimise Si-outdiffusion but is generally high enough for growth of high quality device heterostructures. Doping in one atomic plane made on an arsenic terminated surface is important for certain device heterostructures. Besides the possibility to localise the plane at an arbitrary position in the structure other factors make the δ-doping advantageous over homogeneous bulk doping. The maximum carrier concentration is much higher since the Ga/As-site occupation ratio is enlarged. In addition the mobility is improved at large carrier concentrations because of a spatial electron-donor separation in higher electron subbands as well as screening of impurity charges and high degeneracy of the Fermi-gas. Although the doping is planar during growth on the surface terraces the final embedded doping plane is not perfect. When the GaAs growth is commenced the doping atoms migrate a distance, perpendicular to their initial plane, depending on growth temperature, T_g, and doping concentration, N_{Si2D}. This doping layer thickness increases with growth temperature and its Si-concentration, especially above ~ 550 °C and ~1×10^{13} cm^{-2} respectively. Typical values of thicknesses range from nearly perfect

δ-layers; 5 Å (2 MLs) for $N_{2DSi} = 3.4x10^{14}$ cm^{-2} at T_g = 400 °C to more extended; 30 Å (~ 5 MLs) at T_g = 500 °C for $n_{2D} = 6x10^{12}$ cm^{-2} while 600 °C provides a 180 Å thick doped layer at $n_{2D} = 10^{13}$ cm^{-2}.

The structures were grown by molecular beam epitaxy (MBE) on semi-insulating GaAs (100) substrates using solid source material. A 1 μm thick undoped GaAs buffer layer was grown at 590 °C while the planar doping was performed with open arsenic shutter at ~ 500 °C using the doping furnace under a desired time period. The doping plane was covered by a 0.1 μm thick undoped GaAs cap layer.

The measured free carrier concentration, n_{2D}, was shown to be limited at low and high doping concentrations; N_{Si2D}. No conductivity was detected for $N_{Si2D} = 1.4x10^{11}$ cm^{-2} while $4.3x10^{11}$ only provided 2 % free electrons. Such low carrier concentrations is an effect of the surface depletion field that is emptying the potential of most carriers. Between $N_{Si2D} \approx 2x10^{12}$ and $1x10^{13}$ cm^{-2} the value of n_{2D} is lower than N_{Si2D}. About ~85 % of the dopants provide free electrons at $N_{Si2D} = 7x10^{12}$ cm^{-2} and only ~60 % at $(1\text{-}2)x10^{12}$ cm^{-2}. When the carrier concentration approached $1x10^{13}$ cm^{-2} (0.05 ML) it possessed a slower, non-linear increase with N_{Si2D} followed by a maximum and a saturation which prevailed up to a few MLs. Several factors are limiting the free carrier concentration such as the capture of free electrons in DX- and X-centers. The doping plane results in a V-shaped potential that confine the carriers. The subbands were determined by a self consistent calculation of the Poisson and Schrödinger equations. The main change of the potential is an increasing depth with doping concentration as long the doping plane thickness is limited to 50 Å. Finally we discuss the outdiffusion from the doping plane, the agreement between measured and calculated densities in the V-shaped potential at the δ-plane and the mobility up to a Si-layer thickness of 6 ML. The critical layer thickness of the GaAs/Si/GaAs heterostructure was found to be 3 MLs since 4 ML was relaxed. Above this there were no conduction.

MODIFICATION OF InGaAs/InAlAs HETERO-BARRIERS BY DELTA DOPING

D.W.E. Allsopp, M. Cerniansky[1], M. Hopkinson[2]

Department of Electronics, University of York, England
[1] on leave from the Slovak Technical University at Bratislava
[2] EPSRC III-V Semiconductor Facility, University of Sheffield, England

Unlike metal-semiconductor structures there is, in principle, a choice of barrier height, since the band offsets are determined by the semiconductor alloy compositions. In practice, apart from the $GaAs/Al_xGa_{1-x}As$ system, the range of alloy compositions and hence choice of offset is limited by the requirement for commensurate epitaxial growth in strained layer structures. Lattice mismatch limits the scope for tuning the band offsets of $In_xGa_{1-x}As/In_yAl_{1-y}As$ heterostructures by alloy variation, making alternative methods are desirable.

Capasso and co-workers [1] proposed that the effective band offsets in heterojunctions can be modified by incorporating narrow, heavily doped regions of opposite polarity either side of the hetero-interface during epitaxial growth. A highly localised dipole field then contributes to the potential difference across the junction. The resulting structure, termed the doping interface dipole (DID), has been shown to act as a bias dependent barrier in which the extra dipole contribution to the potential drop across the heterostructure either enhances or opposes the effect of any external bias [2]. In this paper the properties of $In_{0.53}Ga_{0.47}As/In_{0.52}Al_{0.48}As$ DIDs are reported and it is shown that strong modulation of the effective band offset can be obtained.

NIN isotype $In_{0.53}Ga_{0.47}As/In_{0.52}Al_{0.48}As$ heterostructures were grown by MBE on n^+ InP substrates with n^+ and p^+ nominally δ-doped layers situated either side of the hetero-interface, to provide an additional dipole contribution to the variation in electrostatic potential across the heterojunction. The structures were grown with the heterojunction in the middle of a 1 μm wide, nominally intrinsic layer. The n^+ and p^+ δ-doped layers were formed by 5 nm wide regions doped with 2×10^{18} silicon (berylium) impurities/cm^3 set back 20 nm from the hetero-interface, giving an epi-layer structure of 475/5/20 nm undoped/n or p/undoped $In_{0.52}Al_{0.48}As$, followed by 20/5/475 nm of undoped/n or p/undoped $In_{0.53}Ga_{0.47}As$ between n^+ contact layers. The barrier to electron flow is either enhanced or reduced, depending on the order of the n^+ and the p^+ δ-doping. Figure 1 shows schematic band edge variations through the different structures grown.

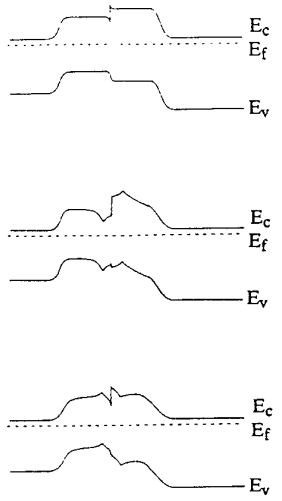


Fig 1 *Schematic band edge variation through heterojunction with and without alternate p^+ and n^+ δ-doping:*
middle structure:enhancing DID;
lower structure: reducing DID.

Figure 2 shows the effect of incorporating an enhancing or a reducing DID on the capacitance-voltage characteristics of NIN isotype $In_{0.53}Ga_{0.47}As/In_{0.52}Al_{0.48}As$ heterostructures.

Without a DID the capacitance is approximately constant with positive applied voltage (reverse bias). Under forward bias the capacitance initially falls, because charge is depleted from the hetero-interface, and then rises again, as the total depletion layer width in the NIN structure decreases. With a reducing DID the C-V characteristic is almost symmetric, with positive and negative applied voltage, accentuating the forward bias behaviour of the basic NIN structure. This occurs because the reducing DID counteracts the diffusion induced dipole typical of a Type I heterojunction. With the enhancing DID the capacitance is constant under reverse bias and

increases monotonically with forward bias. The extra dipole potential from the enhancing DID has caused full depletion of the intrinsic layer.

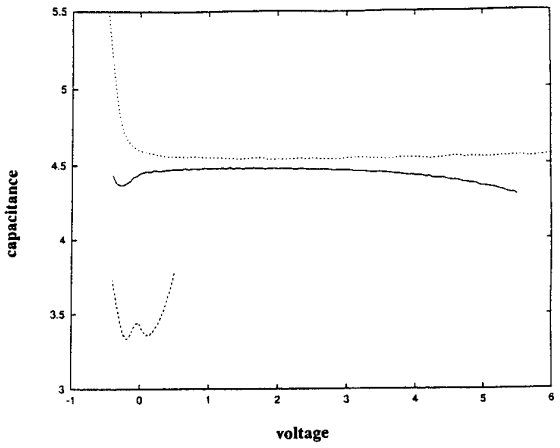


Fig 2 Capacitance-voltage characteristics of NIN isotype $In_{0.53}Ga_{0.47}As$/ $In_{0.52}Al_{0.48}As$ hetero-junction diodes with an enhancing DID (short dashes), a reducing (DID) long dashes) and without a DID (solid line).

Figure 3 compares the forward I-V characteristic at 290K of the basic NIN heterostructure with those containing either an enhancing or a reducing DID. Forward bias is defined in such a way that the current arises from a flux of electrons from the $In_{0.52}Al_{0.48}As$ layer to the $In_{0.53}Ga_{0.47}As$.

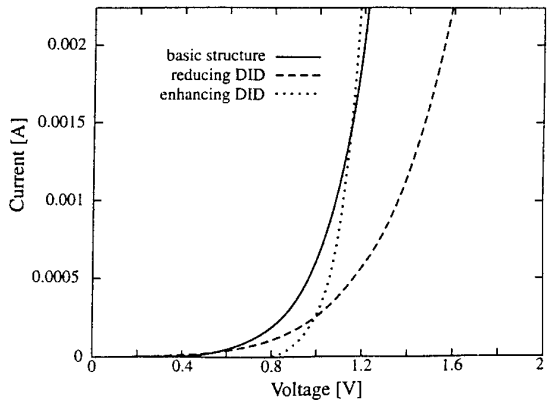


Fig 3 Forward I-V characteristics of NIN isotype $In_{0.53}Ga_{0.47}As/In_{0.52}Al_{0.48}As$ heterojunction diodes with and without DIDs.

In the basic structure forward current is due to both thermionic emission over and from electron tunnelling through the conduction band spike at the hetero-interface. The enhancing DID gives rise to much sharper current turn-on and a smaller ideality factor. The enhancing DID eliminates the conduction band spike via the p^+ δ-doping in the $In_{0.52}Al_{0.48}As$, so that forward current flow is dominated by thermionic emission. Conversely, the reducing DID accentuates the conduction band spike, making forward current predominantly due to electron tunnelling.

The reverse bias characteristics at room temperature of the same three structures are shown in figure 4. As expected enhancing the effective band offset greatly increases the reverse breakdown voltage of the diodes. The structure with a reducing DID shows little difference between forward and reverse bias and gives negligible rectification.

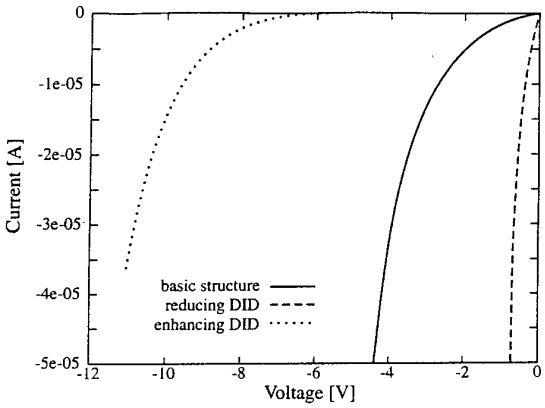


Fig 4 Reverse I-V characteristics of NIN isotype $In_{0.53}Ga_{0.47}As/In_{0.52}Al_{0.48}As$ hetero-junction diodes with and without DIDs.

The viability of using n^+ and p^+ δ-doping to control the potential profile in simple $In_{0.53}Ga_{0.47}As$/ $In_{0.52}Al_{0.48}As$ heterostructures grown by MBE has been demonstrated. In particular, the rectifying properties of NIN heterostructures have been improved using n^+ and p^+ δ-doping, to form a barrier enhancing DID. DIDs can be applied to form injecting contacts with low turn-on voltage (barrier reducing DIDs), or low leakage, higher breakdown voltage junctions (barrier enhancing DIDs).

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NEW ELECTRONIC MATERIALS: LOW TEMPERATURE GROWN GaAs AND InP

W.M. Chen, E. Sörman, B. Monemar
Department of Physics and Measurement Technology
Linköping University, S-581 83 Linköping, SWEDEN

P. Dreszer, A. Prasad, X. Liu, E.R. Weber
Department of Materials Science and Mineral Engineering,
University of California and Center for Advanced Materials,
Lawrence Berkeley Laboratory, Berkeley, CA 94720, USA

B.W. Liang and C.W. Tu
Department of Electrical Engineering,
University of California at San Diego, La Jolla, CA 92093, USA.

Non-stoichiometric semiconductors grown by modern growth techniques, such as GaAs and InP thin films grown at low-temperature (LT) by molecular beam epitaxy (MBE), have attracted increasing attention due to their fascinating physical properties and have opened new directions for device applications. However the physical properties of these materials, including many key questions to a full exploration of device applications, are still poorly understood.

In this work we have investigated electronic and transport properties of these modern electronic materials as well as the role of defects in controlling these properties by various experimental techniques, such as Hall effect measurements, deep level transient spectroscopy (DLTS), optical absorption, magnetic circular dichroism of absorption (MCDA), and optical detection of magnetic resonance (ODMR). External perturbations such as hydrostatic pressure and magnetic field were also employed for a better understanding of the physical properties. Exciting progress has recently been made in the understanding of interesting new materials such as low-temperature MBE-grown InP and GaAs thin films. We have revealed the dominant mechanisms responsible for the semi-insulating properties of LT-GaAs and for the metallic conductivity of LT-InP and have therefore resolved one of the main controversies in the field.

Highly As-rich LT-GaAs grown below 400 °C has attracted great attention in recent years, because of unique properties such as record-high resistivity, extremely short carrier lifetime and yet a reasonably good mobility. These non-stoichiometrically grown materials provide new possibilities for a wide variety of promising applications as buffer layer offering superior device isolation and very high breakdown voltage, as gate contact isolation layer and as active layer in photoconductive switches yielding transient times in the fsec range (i.e. in

the THz range). There exist, however, controversial models to account for the SI properties of the annealed LT-GaAs, as due to the residual As_{Ga} defects or the As precipitates. In this work we determine the concentration of As_{Ga} defects in neutral and positive charge states, As_{Ga}^0 and As_{Ga}^+, by near-infrared optical absorption and MCDA. We found that a high concentration of the defects is always present in the LT-GaAs studied, with the concentration of As_{Ga}^0 larger than that of As_{Ga}^+ defects. This result indicates that the defects can account for the pinning of the Fermi energy, and consequently also the semi-insulating properties. This work not only resolves the controversy for the SI properties of LT-GaAs, but also points to the direction to achieve new type of SI GaAs with superior properties as well as good material quality.

There has been a continuous effort in searching for methods to produce undoped semi-insulating (SI) InP, as a desirable substrate material or for device isolation in InP-based optoelectronics. The SI behaviour of LT-GaAs, which is highly As rich, has inspired an effort to grow InP at low temperature under phosphorus over-pressure in the attempt to achieve undoped SI InP. Very unexpected and surprising results were observed in this work, however, as as-grown LT-InP was shown to be highly n-type conductive. The electron concentration was shown to increase dramatically with decreasing growth temperature. At low growth temperatures below 350 °C, metallic-like electrical transport indicated that the electrons formed a degenerate gas in the conduction band. Using high-pressure Hall effect measurements, we have found that the electronic transport in LT-InP is determined by the presence of the dominant deep donor level which is resonant with the conduction band located 120 meV above the conduction band minimum.

To identify the defects present in LT-InP, in particular those governing the electronic properties, we carried out a detailed study by the microscopically informative ODMR technique. The presence of the P_{In}-antisites is unambiguously established, evident from the doublet hyperfine structure from the ^{31}P atom (with nuclear spin I=1/2 and 100 % natural abundance). The P_{In}-antisites are shown to be involved in strong non-radiative recombination processes. Photo-excitation of the P_{In}-antisite ODMR signal allows determination of the (+/++) energy level position to be at about 0.23 eV below the conduction band, consistent with the results from Hall effect measurements and DLTS.

We have shown with correlated optical and electrical measurements that the P_{In} antisite is the prevailing defect in LT-InP. The increase in free-carrier concentration (monitored in Hall effect measurements) correlates very well with the increase in the P_{In}^+ concentration (monitored by MCDA of P_{In}^+), with decreasing growth temperature. The dominant deep donor level at $E_C + 0.12$ eV in LT-InP is therefore shown to correspond to P_{In} (0/+). It is the auto-ionization of the P_{In} antisite via its first ionization stage which leads to the n-type conductivity in as-grown LT-InP. This work therefore concludes that the introduction of P_{In} antisites in InP is not at all suitable to achieve SI material, and has resolved the puzzle in materials science of LT-InP.

SESSION 2

OPTOELECTRONIC DEVICES I

Semiconductor Laser Reliability

Mitsuo Fukuda
NTT Opto-electronics Laboratories
3-1, Morinosato Wakamiya, Atsugi-shi, Kanagawa, 243-01 Japan

Semiconductor lasers have been widely applied in many fields from optical transmission systems to consumer electronics, such as compact disks. In those systems or equipments, especially for the optical fiber transmission systems, high performance and high reliability are strongly required. Therefore, the reliability has been mainly improved for lasers used in the transmission systems. There are two types of lasers used in such systems, AlGaAs/GaAs lasers and InGaAs(P)/InP lasers including multi-quantum well (MQW) and strained MQW structures.

The basic degradation mechanisms are summarized in Fig. 1 for AlGaAs/GaAs lasers, and in Fig. 2 for InGaAs(P)/InP lasers [1]. These mechanisms are governed by the properties of the materials used. AlGaAs/GaAs is very sensitive to defects. Through nonradiative recombination processes, several kinds of dislocations are generated and grow during operation. In addition, the rate of nonradiative recombination at the mirror facet is high. Thus the facet oxidation (photo-enhanced oxidation) and catastrophic optical damage (COD; melting of facet) occurs easily at a low output power level. These degradations are suppressed or eliminated by improving crystal quality and employing some facet passivations. InGaAs(P)/InP, by contrast, is insensitive to defects. Consequently, the inner region and the facet is quite stable during operation.

Degradations at electrodes and bonded parts are common for both types of lasers. The rate of degradation is also determined by the material used. A Schottky-type electrode, such as Ti/Pt/Au, is stable when compared with alloy type electrodes. No degradation is often observable. In Figs. 1 and 2, electrode degradation for only alloy-type electrodes is indicated. For bonding metals, a long-term stability has been obtained by using hard solders with high melting temperatures.

The degradation mechanisms for lasers composed of bulk and MQW structures are barely different. In strained (M)QW lasers, a strain of about 10^{10} dyn/cm^2 at the active region causes new degradation modes. A typical one is facet degradation in 0.98-μm InGaAs/AlGaAs lasers. The inner region of these lasers is quite stable, but the facet is easily oxidized, if it is not coated with a dielectric film. COD is generated at a relatively low output power level. The trigger of the facet degradation is the band gap shrinkage due to the release of strain at the facet, because the strain changes from biaxial in inner region into uniaxial at the facet. A positive feedback loop of the facet degradation in 0.98 μm lasers is shown in Fig.3 [2]. These degradations can be suppressed by suitable

passivations.

As described above, various kinds of degradation modes have been observed, and suppressed or eliminated in semiconductor lasers. Consequently, these lasers have device lives more than 10^5 hours under practical operating conditions in systems or other equipment.

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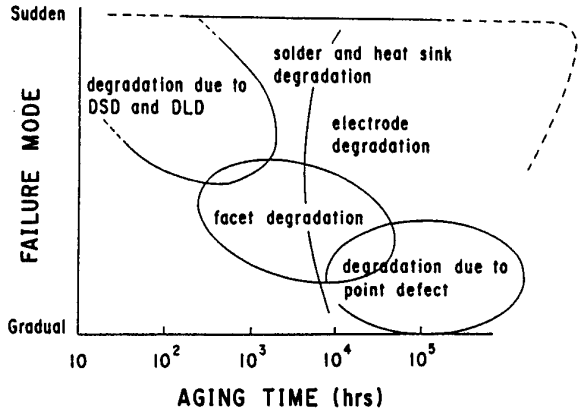

Figure 1 Estimated degradation modes under practical operating conditions for AlGaAs/GaAs lasers. DSD and DLD expresse a dark spot defect and a dark line defect, respectively.

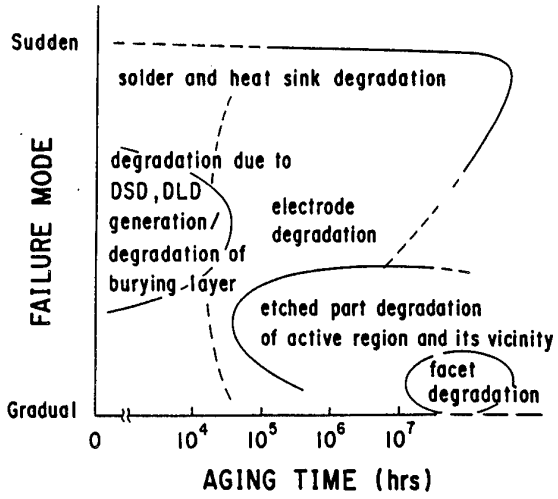

Figure 2 Estimated degradation modes under practical operating conditions for InGaAs(P)/InP lasers.

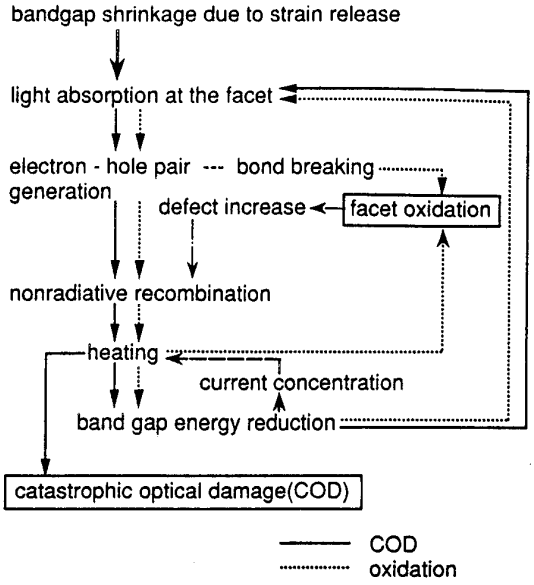

Figure 3 A feedback loop of facet degradation in 0.98 μm-strained QW lasers.

RELIABILITY OF MOCVD GROWN AlGaInP SURFACE EMITTING LEDS

D. V. Morgan, Y. H. Aliyu and H. Thomas

Department of Electronics School of Engineering, University of Wales College Cardiff,

P. O. Box 917 Cardiff UK CF2 1XH

High brightness semiconductor light emitting diodes and laser are key components in optoelectronic application. Combination of LEDs in a hybrid or monolithic form are the competitors for the lucrative visible aplha-numeric display market. These sources have also been used as sources in various kinds of optical transmission system. Recently quaternary AlGaInP have been investigated for optical device applications in the visible spectral region. These studies include lasers[1] and LEDs[2]. AlGaInP has a wide bandgap in which direct energy transitions occur in the spectral region between green and orange. This material system have exhibited high brightness LEDs ranging between red to green. AlGaInP LEDs enable LEDs to be used for applications that require either high output power or low power consumption. The reliability of optical sources is strongly dependent on the degradation mode and device characteristics such as current versus optical power and its temperature dependence[3]. The mechanism of efficiency degradation of these LEDs is not fully understood. Increase of non-radiative centres, generation of crystal defects and surface effects might be possible sources.

This paper reports on the preliminary life testing of orange, yellow and green AlGaInP LEDs under the condition of thermal and electrical stressing. The objective being two fold: (i) To estimate the operational life mean life to failure and (ii) when failure occurs to identify the basic physical mechanism responsible. The characterisation techniques used are Current-Voltage(I-V), Capacitance-Voltage(C-V), Deep Level transient spectroscopy (DLTS), Light-Current (L-I) and Spectral Response(R-S) are used characterise the LEDs. Reliability studies at constant driving current of 50 mA and 100 mA were conducted at temperature range from 20°C to 100 °C. Initial light output characteristics showed a slight increase before starting to

degrade for the orange and yellow devices. This is attributed to the annealing effects of defect levels. The light output of the green LEDs degraded to less than 50% of the original output after 175 hours, after which all the devices exhibit a similar pattern of degradation.

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Photoluminescence study of carrier transport in InGaAsP quantum well laser structures

S. Marcinkevicius,[a] U. Olin,[b] C. Silfvenius,[c] B. Stålnacke,[c] J. Wallin,[c] and G. Landgren [c]

a) Department of Physics II, Royal Institute of Technology, S-100 44 Stockholm, Sweden

b) Institute of Optical Research, S-100 44 Stockholm, Sweden

c) Semiconductor Laboratory, Royal Institute of Technology, Electrum 229, S-164 40 Kista, Sweden

Intrinsic limitations of high-frequency characteristics for quantum well (QW) lasers are set by the time of carrier transfer from the contact layers to the QW layers from which the lasing occurs. There are several physical processes involved in the carrier transfer, such as carrier transport in the confinement layers, carrier cooling, carrier capture, etc. Though in the operating lasers these processes take place simultaneously, their division and separate investigation is useful for a better understanding of carrier transfer, and for modelling of the laser structures with improved characteristics.

Time-resolved photoluminescence (PL) is an experimental technique widely used in the studies of non-equilibrium effects in semiconductor nanostructures. The PL signal is proportional to the product of electron and hole densities, and can be used to monitor temporal changes in these densities. In the present work we show that by using time-resolved PL spectroscopy and choosing appropriate design of the QW laser structures, it is possible to distinguish and study separately such carrier transport processes as electron and hole transport in the confinement layers, electron capture into the QWs, and electron redistribution between the QWs. Since these effects occur on picosecond and even subpicosecond time scales, high temporal resolution of the measurements is required. We satisfy these requirements by using a femtosecond Ti:sapphire laser which generates pulses of 100 fs duration, and a photoluminescence upconversion technique [1]. The temporal resolution for such measurements is ~150 fs.

Fig. 1 shows a band gap profile of a typical laser structure used in the investigations. The grading of confinement region is accomplished in several steps using InGaAsP layers of different composition, lattice matched to InP. The variation of geometrical parameters and doping levels of the structures allows us to set experiments in which different carrier transport effects can be studied.

Ambipolar carrier transport (determined by the slower holes) in the confinement layers has been studied by using high intensity photoexcitation, so that excited carrier density is much higher than the doping level of the structure layers. The carriers have been excited mainly in

the top InP layer, and their movement towards the active region containing QWs has been monitored by measuring PL transients at energies corresponding to the band gaps of the different steps. PL rise (decay) times can be associated with the times when a carrier packet arrives to (leaves) a certain layer. A typical example of such PL transients is shown in Fig. 2. It has been found that ambipolar carrier transport proceeds with a constant velocity of 1.5×10^6 cm/s and can be explained by a step-driven diffusion model [2].

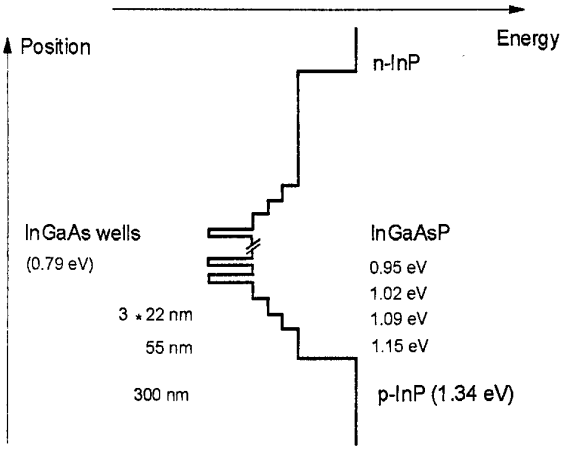

Figure 1. *Band gap profile for the investigated laser structures.*

To study electron transport, we have used highly *p*-doped structures and maintained the photoexcited carrier density well below the doping level. The time for the electrons to transfer over one step has been found to be no more than 250 fs, and the electron transport mechanism in the confinement layers is hot electron diffusion [3].

Electron capture into the QWs has been studied by using the structures with a thin top InP layer, so that most of the carriers are excited in the confinement region. Under such conditions, changes in the PL spectra reflect electron cooling in the confinement layers and electron capture into the QWs. A characteristic time constant for the electron capture is 1.4 ps.

And finally, if a structure is modified so that a deeper well is introduced at one side of the active layer, time-resolved PL allows to study vertical carrier transport in the QW region. We have found that for 5 nm thick barriers between the QWs, the electron diffusion proceeds through the miniband with a diffusion coefficient similar to that of the equivalent alloy.

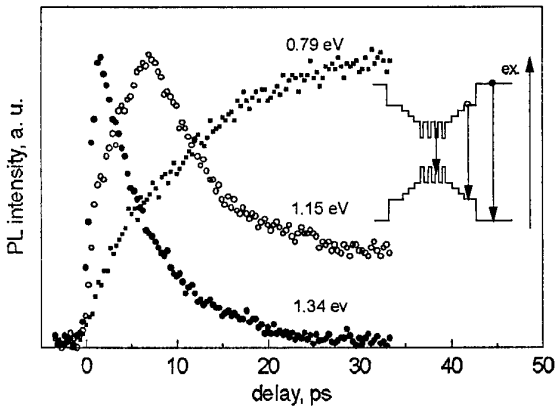

Figure 2. *Temporal behaviour of the photoluminescence signals, under ambipolar transport conditions, for photon energies corresponding to the layers indicated in the inset band gap structure.*

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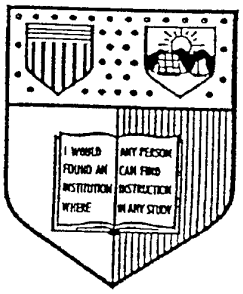

Temperature Effects on the Performance of High Speed Quantum Well Lasers

Robert M. Spencer*, Sean S. O'Keefe*, Chin-Yi Tsai†, Joseph Greenberg†, Jürgen Braunstein¥, Glenn H. Martin*, William J. Schaff*, and Lester F. Eastman*

* School of Electrical Engineering and the National Nanofabrication Facility
Cornell University, Ithaca NY 14853

† School of Applied and Engineering Physics and the National Nanofabrication Facility
Cornell University, Ithaca NY 14853

¥ Fraunhofer-Institut für Angewandte Festkörperphysik
72 Tullastraße, D-79108 Freiburg, Germany
current address: School of Electrical Engineering, Cornell University, Ithaca NY 14853

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Optimization of the optical guide design and cavity design of multiple quantum well lasers for efficient microwave optical links

Robert M. Spencer*, Sean S. O'Keefe*, Chin Yi Tsai†, Joseph Greenberg†,
Jürgen Braunstein¥, Glenn H. Martin*, William J. Schaff*, and L.F. Eastman*

*School of Electrical Engineering, Cornell University, Ithaca, NY 14853

†School of Applied and Engineering Physics, Cornell University, Ithaca, NY 14853

¥Fraunhofer-Institut für Angewandte Festkörperphysik, 72 Tullastraβe, D-79108 Freiburg, Germany
current address: School of Electrical Engineering, Cornell University, Ithaca, NY 14853

Abstract

We show the results of an experimental and theoretical investigation into the present limitations on the overall small signal direct modulation bandwidth in semiconductor lasers. The influence of the optical guide design and cavity design is examined.

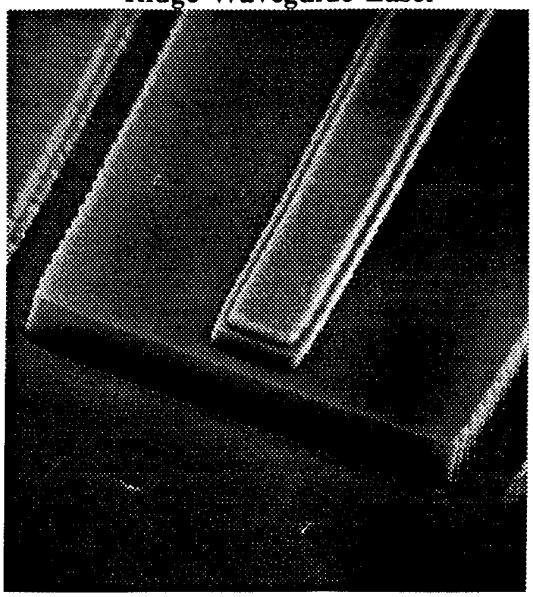
The modulation bandwidth is a measure of the ability of the optical output of a semiconductor laser to follow the electrical input current. Therefore, any delay in the process where an electron-hole pair is injected into the device until it is felt as the output of a photon from the cavity limits the overall high frequency performance of the laser. A small signal analysis of this problem must consider all of these delays and not assume that injected carriers are instantaneously available in the gain region where they may participate in stimulated emission. It is now well established that a consideration of these delays introduces additional terms in the damping rate that must be considered. Two of the most important mechanisms that inhibit the resonance frequency and increase the damping rate are:

(a) The carrier transport/capture/escape parameter

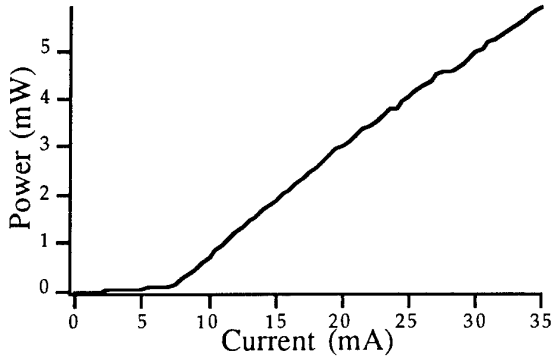
(b) The energy relaxation rate determined primarily by the ability of LO phonons to remove energy from carriers and then decay into acoustical phonons that transmit this energy away from the active region of the device

Strained layer quantum well lasers were fabricated using molecular beam epitaxy (MBE), e-beam lithography, and chemically assisted ion beam etching (CAIBE). Single-sided output cavities are demonstrated using a total internal reflector at the end of the cavity in conjunction with a standard plane mirror. Carrier transport issues are examined by comparing a gain region with the quantum wells centered in the optical guide with a gain region where the quantum wells are offset toward the p-cladding. In addition, the effect of uniformly doping the active region is studied. DC, spectral, and microwave comparisons of the various structures are shown. Threshold current for 4 quantum well material as low as 8 mA are shown and -3dB modulation bandwidths of 19 GHz are shown for extremely low bias currents of 24 mA. Future challenges in directly modulating semiconductor lasers are presented, as well as possible solutions for devices suitable for use in a wide variety of microwave optical links.

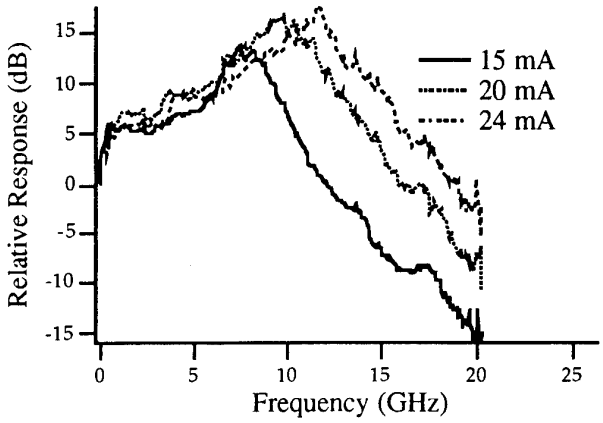
Ridge Waveguide Laser



Optical output power vs. current for a 3 μm x 75 μm ridge waveguide laser



Relative modulation response of a 3 μm x 75 μm ridge waveguide laser



Improved Design for 4x4 Integrated InP Switch Matrices with Butt Jointed Semiconductor Optical Amplifier Gates

W. van Berlo, M. Janson, M. Gustavsson, J. Terlecki, P. Granestrand, A.-C. Mörner, J.-E. Falk
Ericsson Components AB, Isafjordsgatan 16, S-164 81 Kista, SWEDEN

The fabrication of 4x4 integrated InP switch matrices with butt jointed optical amplifiers is presented in detail. The results show an improved fibre-to-fibre gain and polarisation independence over the previous design as well as a better uniformity in gain and extinction ratio.

Introduction

Switch matrices with integrated optical amplifier gates play an important role in the realisation of optical transparent transport and access networks. They have received considerable interest over the years and several designs have been demonstrated [refs 1-3]. The advantage of using integrated semiconductor optical amplifiers in the matrices is their compact size which allows for smaller components, and their potential use as reverse or forward biased detectors.

In previous publications we have reported on the design, manufacturing and characterisation of switch matrices with integrated amplifiers [refs 1,4]. A problem in this original design was the polarisation dependence of the amplifiers and the coupling efficiency between the passive and active waveguides. Polarisation dependence was estimated to be in the range 6-12 dB, at a fibre-to-fibre gain of approximately -5 to 0 dB. In this paper we present a new integration scheme and waveguide design which leads to an improved polarisation independence and higher gain.

Main characteristics of the new design are:

1 better coupling between passive and active waveguide sections;
2 less critical processing;
3 better control of active layer linewidth due to a single dry etch step (compare: dry etch and wet etch in the previous design);
4 shorter gate lengths needed due to higher confinement factor in the new design. The higeher confinment factor however, also leads to increased gain saturation of the optical amplifiers.

Process

The process for the switch matrix with butt joint coupled waveguides is based on the previous process design. The main differences are the waveguide coupling and the use of e-beam lithography for waveguide definition. The new coupling scheme should lead to an improved insertion efficiency between the passive and the active waveguide, while e-beam lithography is necessary for controlling the narrow linewidths which are needed for polarisation independence.

The basic structure consists of a 0.5 μm thick InGaAsP active layer (PL wavelength = 1.55 μm) and a p-type contact layer. The structure is grown by Metalorganic Vapour Phase Epitaxy (MOVPE), as are all subsequent semiconductor layers. The active regions are defined by optical lithography and etched by reactive ion etching (RIE), using a methane/hydrogen gasmixture The butt joint integrated passive waveguide structure consists of a 0.6 μm thick InGaAsP layer with a PL wavelength of 1.3 μm. After regrowth, the waveguide structure is defined by e-beam lithography and etched by RIE. The waveguides are typically 0.6 - 0.7 μm wide. After etching of the waveguides, the active regions are defined once more and current blocking layers (InP:Fe) are regrown selectively. The regrowth mask is then removed and contacting layers are grown over the whole structure. Metalisation of Au/Zn contacts is done and contacts are defined by optical lithography. Finally the backside is polished to about 150 μm and metalised (alloyed AuGeNi contacts).

Cleaved chips are mounted face up on silicon carriers for analysis and face down (flip chip) for packaging. All chips are antireflectance coated before testing and packaging.

Results and dicsussion

Gain curves of a typical switch are shown in figures 1a and 1b, for both polarisations. The figures show the gain characteristics of a typical switch route. For figuer 1a, the gate switch current was varied from 0 to 50 mA while the in- and output amplifiers were kept at a constant drive current of approximately

20 mA each. The fibre input power was -20 dBm at a signal wavelength of 1.558 μm, while the temperature was kept constant at 25 °C. As can be seen from the figure, the polarisation dependence is minimum, which was the main objective of this redesign.
Figure 1b shows the gain saturation characteristics of the switch (one route). The active sections (input, gate and output) were kept at a constant current of 16 mA each, while the input power was varied. The signal wavelength in this case was 1.567 μm. The low saturated power of about -18.5 dBm is due to several factors, e.g. the high confinement factor (approximately 0.6) and possibly a less efficient current injection with an associated lower population inversion of the narrow amplifier waveguide [ref 5].

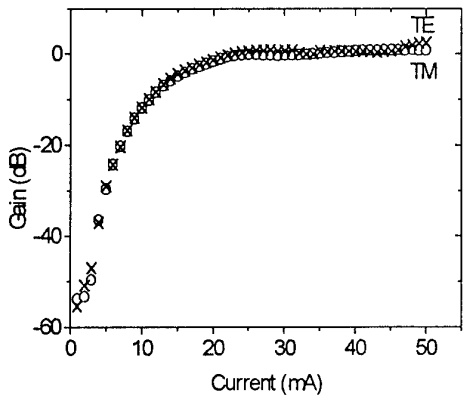


Figure 1a

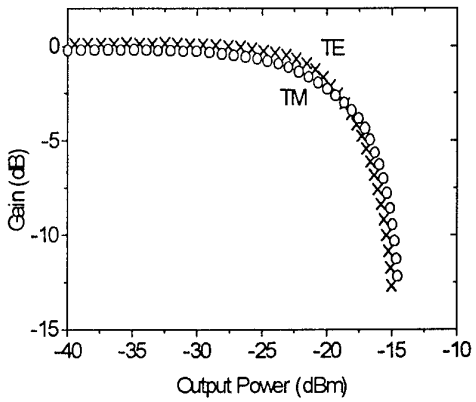


Figure 1b

The maximum fibre-to-fibre gain of the device varied from -5 to 2 dB between all possible paths. The extinction ratio was between 30 and 60 dB, with only one path having a lower extinction ratio (25 dB).

Acknowledgements: This work was in part performed within the RACE 2028 (MWTN) project.

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OPTOELECTRONIC INTEGRATED CIRCUITS BASED ON COMMERCIALLY PROCESSED GaAs IC's

Clifton G. Fonstad

Department of Electrical Engineering and Computer Science
National Center for Integrated Photonics Technology
Massachusetts Institute of Technology
Cambridge, MA 02139

This presentation will describe a technology being developed for creating optoelectronic integrated circuits (OEIC's) containing VLSI-density and -complexity electronic circuitry integrated with a full range of active and passive optoelectronic devices. This technology builds upon established commercial GaAs integrated circuit processes and involves epitaxially growing GaAs-based heterostructures on fully-metalized VLSI-level GaAs integrated circuit wafers. These heterostructures are subsequently processed to create various optoelectronic devices monolithically interconnected with the pre-existing electronic circuitry to yield completed monolithic OEIC's of unprecedented complexity.

This technology -termed epitaxy-on-electronics, or "epi-on-electronics" for short - offers an immediate path to complex, high performance OEICs and has already been demonstrated in a number of circuits which involve the integration of light emitting diodes, and m-s-m and MESFET photo-detectors, with novel network decision circuits and with digital switching circuits. A multi-investigator team within the National Center for Integrated Photonic Technology (NCIPT) is working to expand the menu of optoelectronic devices available for integration (to include surface-emitting lasers, photodiodes, modulators and SEEDs, and waveguide devices), as well as to increase the scope of applications for epi-on-electronics OEICs, and to make the technology available to the user community.

Fabrication of and Photoluminescence from InGaAsP microdisks

B. Corbett, J.Justice, L.Considine, S. Walsh and W.M.Kelly
National Microelectronics Research Centre, University College Cork, Ireland

Microcavities present an attractive alternative to electronic confinement in the quest to demonstrate atomic-like features in the semiconductor environment. The dimensional requirement on photonic confinement is relaxed compared to that for electrons. One dimensional mode control utilising multilayer Bragg mirrors are familiar in vertical cavity lasers. As in the transition to quantum wires and dots, three dimensional confinement of photons in semiconductor structures poses many practical difficulties. The microdisk presents a structure which is inherently three dimensional. Spontaneous emission into radiation modes is inhibited while high coupling efficiency of the emission into whispering gallery modes which propagate along the disk boundary have been predicted and measured.

We have developed an unique microdisk fabrication technology which uses in various measures the techniques of epitaxial lift-off, metallic bonding and wet etching. These techniques allow the fabrication of novel microdisk geometries which address the issues of optical mode confinement, heat sinking and possible directional control of the emitted light. Disks with diameters between 2 and 8μm have been fabricated in the InP/InGaAsP material system. The structures include disks with InP and SiO_2 pedestals and with silicon and metallic coated substrates.

Photoluminescence spectra have been measured at 77K under cw optical pumping. The microdisks on glass substrate/pedestals present the most interesting results as the higher mode confinement has allowed the measurement of the radial mode structure. This is in contrast to the reports in the literature where only the lowest order radial modes have been observed due to coupling into the substrate via the high refractive index pedestal. Figure 1 presents the spectrum from a 6μm diameter disk composed of a separate confinement heterostructure with room temperature emission at 1.32μm. Figure 2 is the lasing spectrum from a 7μm diameter InGaAsP microdisk of 160nm thickness (λ_{gap} 1.55μm at 300K) well above threshold. Several lasing modes are observed. Mode competition is measured with increasing pump powers.

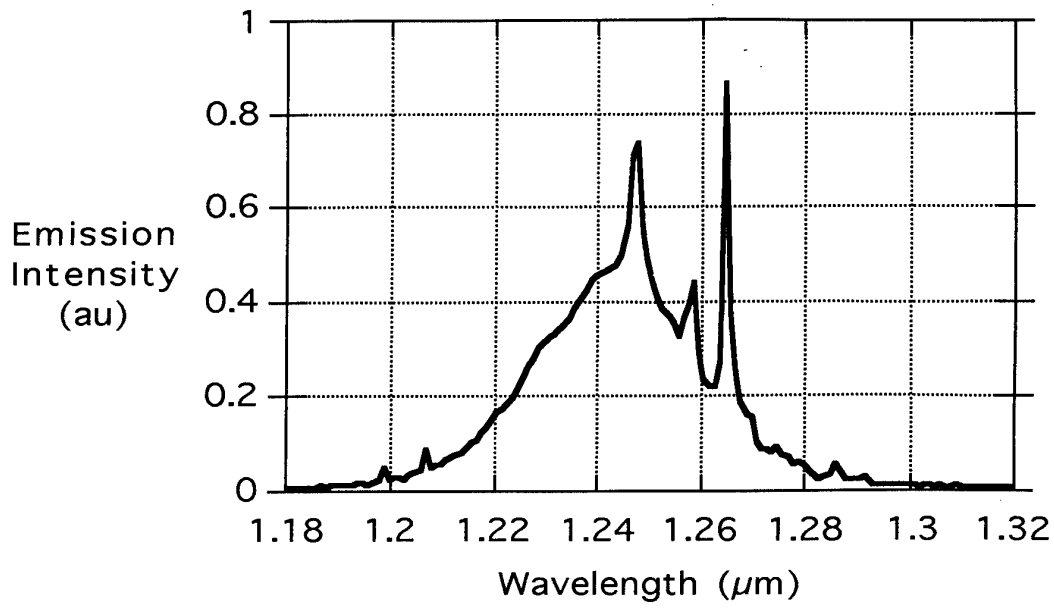

Figure 1: Emission spectrum at 77K from a 5μm diameter microdisk suspended on a glass layer when pumped below threshold

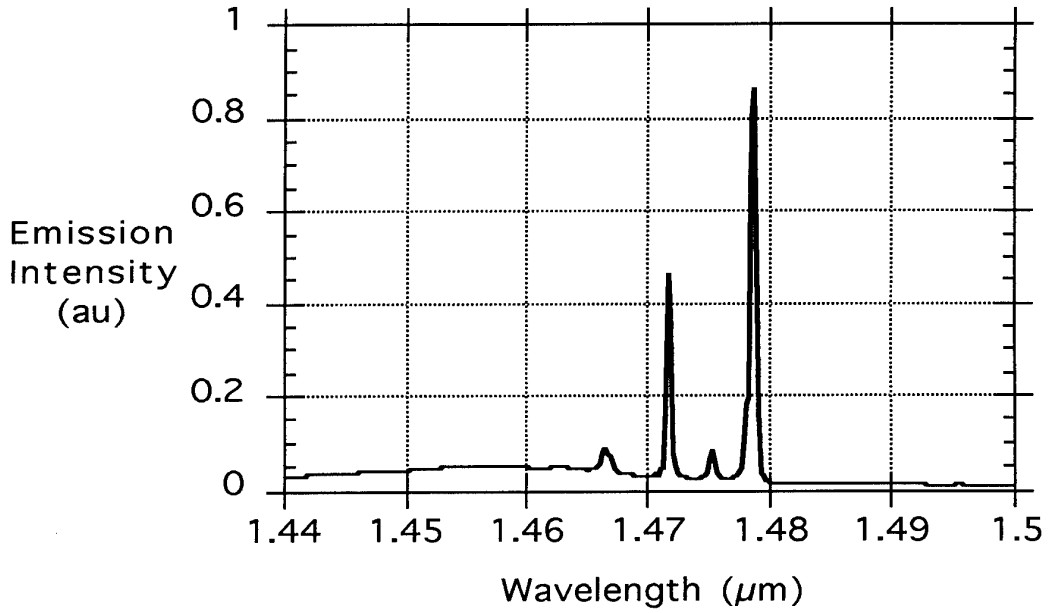

Figure 2: Lasing spectrum at 77K from a 7μm InGaAsP disk suspended on a glass pedestal.

Confinement effect on excitons in self-organized InGaAs quantum disks

H. Weman,[1] H. Kamada,[2] M. Potemski,[3] J. Temmyo,[2] R. Nötzel,[2*] and. T. Tamamura[2]

[1]Department of Physics and Measurement Technology, Linköping University, S-581 83, Linköping, SWEDEN
[2]NTT Opto-electronics Lab, 3-1 Morinosato, Atsugi, Kanagawa, 243 01, JAPAN
[3]High Magnetic Field Laboratory, MPI/FKF and CNRS, F-38042 Grenoble, FRANCE

ABSTRACT

Recently there has been a large interest in self-organized formation of quantum dot structures through a controlled islanding during the growth of highly strained quantum well films, however in most cases with low ordering and low density of the dots. We have found that well ordered, high density dot arrays can be formed during spontaneous reorganization of a sequence of AlGaAs and strained InGaAs epitaxial films grown on GaAs (311)B substrates by MOVPE.[1] The size of the quantum disks are as small as 20 nm, and the photoluminescence is characterized by narrow linewidths and well resolved exciton resonances in excitation spectroscopy. Laser structures with double stacked quantum disks as active layers have shown room temperature CW operation with low threshold currents, indicating the potential for opto-electronic device applications.[2] Here we report on the high-field magneto-luminescence experiments of InGaAs quantum disks for various sizes, to systematically investigate lateral confinement effects on the excitonic properties of the disks. The circularly polarized excitation spectra for these disks were measured in the Faraday configuration, in fields up to 20 Tesla. To increase the resolution of our measurements we also measured the circular polarization spectrum directly using a photo-elastic modulator. Starting from about 5 Tesla we see several higher Landau levels in the disks with the number of levels depending on the size of the disk. Above 10 Tesla the magnetic confinement starts to dominate and there is not much difference in the Landau-level energy spectrum between a disk and a reference quantum well sample. We have calculated the binding energy for excitons confined in a (311) quantum well and (311) quantum disk (including lateral confinement). We see a systematic increase in the exciton binding energy for smaller disks, increasing from about 8 meV for the large disks to about 20 meV for the smaller disks. Part of this enhancement is caused by the enhanced electron-hole Coulomb correlation due to the lateral confinement, but some is also caused by the enlarged in-plane hole mass as a result of inter-valence band mixing due to the (311) in-plane biaxial strain.

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* Present address: RCIQE, Hokkaido University, N13, W8 Sapporo, Hokkaido 060, Japan

SESSION 3

OPTOELECTRONIC DEVICES II

Long Wavelength Vertical Cavity Surface Emitting Lasers

Klaus Streubel, Anders Karlsson, Sebastian Lourdodoss, Jörn Dechow, Magnus Höijer, Thomas Heide and Gunnar Landgren

Laboratory of Photonics and Microwave Engineering, Department of Electronics, Royal Institute of Technology, Electrum 229, S-164 40, Kista, Sweden

Abstract:

We review the progress of realizing room temperature continous wave electrically pumped long wavelength vertical surface emitting lasers.

Vertical cavity surface emitting semiconductor lasers (VCSELs) are very promising as low cost light sources due to the small volume leading to a low threshold, the vertical geometry with an active region inside the chip edges giving an expected increase in reliability and uniformity, the improved beam quality relaxing fiber coupling tolerances, as well as the possibilities for array integration.

Progress in short wavelength (0.85 μm and 0.98 μm) VCSELs has been rapid in the last few years, i.e. thresholds of 50 μA [1], power conversion efficiences of 50 % [2] and device yields of 99.8% across a 3" wafer [3] have all been reported. Recently, commercial VCSEL arrays also reached the market.

However, at long wavelengths, i.e. 1.3 μm and 1.55 μm, progress has not seen such a rapid pace. So far, the highest operating temperature of CW electrically pumped VCSELs at 1.3 μm is 14°C [4], and at 1.55 μm only pulsed room temperature lasing has been reported [5-7]. The reason for this lies in the lack of availability of materials for the fabrication of Bragg mirrors, and in the non-linear (Auger) recombination at long wavelengths, both leading to large threshold current densities and hence problems with heat removal. Semiconductor mirrors of InGaAsP/InP, the material of the active layer, suffers from a small refractive index step, and hence many mirror periods ≈40-50 are needed to achieve a large reflectivity > 99 %. To get around having two thick epitaxial mirrors, one [5] or two [4] dielectric mirrors, single [6] or double wafer fused GaAs/AlAs [7] mirrors have been employed.

In the talk, we will discuss basic VCSEL properties, review european and worldwide activities in long wavelength VCSELs, discuss the applications of long wavelength VCSELs, and in some detail discuss our results obtained so far on optical pumping (equivalent $J_{th} \approx 2$ kA/cm^2) MOVPE grown 1.55 μm VCSELs.

Financial support from the Swedish Board of Technical Devolopment (NUTEK) and the Technical Sciences Research Council (TFR) is acknowledged.

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VERTICAL CAVITY SURFACE EMITTING LASER CHARACTERIZATION BY PHOTOREFLECTANCE SPECTROSCOPY.

P.D. Berger*, C. Bru*, T. Benyattou*, G.Guillot*, A Chenevas-Paule**, P. Grosse**

* Laboratoire de Physique de la Matière, INSA de Lyon-(URA CNRS 358)
Bât 502, 2ème étage, 20, avenue A. Einstein, 69621 Villeurbanne Cedex. FRANCE

** LETI (CEA - Technologies Avancées) Dept OPT-CENG
17, rue des Martyrs, 38054 Grenoble Cedex FRANCE

Vertical cavity surface emitting lasers (VCSEL) have several well known advantageous properties, including single longitudinal mode operation, small beam divergence, low threshold current, and ease of integrability. However, such structures require a good thickness homogeneity, and non destructive characterization is necessary prior to full processing in order to provide confirmation of the good quality of epitaxial structure. We have studied top surface emitting structures, centered near 800nm with a lamba cavity, in the GaAs/AlGaAs system, grown by gas source Molecular Beam Epitaxy (GSMBE). Our epitaxial process gives good thickness uniformity over 3 inch wafer. Measurements of the reflexion coefficient versus wavelength are realized by multichannel reflectivity in the GSMBE introduction chamber.

Experimental studies are undertaken on two samples: one is a typical top emitting VCSEL structure and the other one (incomplete) consists of the distributed Bragg reflector (DBR) n^+ bottom mirror and the cavity (including GaAs quantum well) without the DBR p^+ top mirror. Structures are characterized by photoreflectance (PR) spectroscopy under normal incidence. This technique offers a unique non invasive opportunity to check the quantum well alignment with the cavity mode, through the comparison of PR spectra and reflected signal. This allows a particularly good observation of the Fabry-Pérot cavity mode (finesse and position) and points out the cavity properties.

A PR study of the full structure shows that the quantum well transition is drastically reduced in the wavelength range where the reflexion coefficient is very high. In order to be able to observe the quantum well transition, we have artificially placed it in the neighbourhood of the cavity resonance mode where R is reduced : we have performed PR experiments at lower temperatures (down to 9K). This is expected to increase the energy of the quantum well transition as the temperature is decreased, while the cavity bandpass does not shift as much. As expected, a PR feature is arising in the wavelength range corresponding to the cavity mode and its intensity is

maximum at 110K. Under normal incidence, the number of reflexions within the cavity increases, which enhances the PR signal.

The PR spectra exhibit Franz-Keldysh oscillations above AlGaAs band gap from which the electric field within the cavity is determined, and goes from 17kV/cm at 9K up to 38kV/cm at room temperature due to a reduced photovoltage effect.

Results at room temperature from the incomplete structure give the real Al composition of the barrier material in the cavity in good agreement with the nominal one. It determines as well the transition energies from the quantum well without any high reflexion coefficient problems.

This work gives the proof of the unique potentialities of PR experiments for the VCSEL characterization and their GSMBE growth calibration.

Heavily C-Doped GaAs/AlGaAs Multi-Quantum-Well Normal Incidence Infrared Photodetectors

E. Mao, B.W. Kim, Z.H. Lu, S.A. Dickey, and A. Majerfeld
Department of Electrical and Computer Engineering, CB425
University of Colorado, Boulder, CO 80309. USA

Normal incidence Multi-Quantum-Well (MQW) photodetectors are attractive for focal plane infrared (IR) detector arrays. In this work, we show experimentally that normal-incidence absorption coefficients of over 10^4 cm^{-1} can be achieved in the 10 μm wavelength range for p-GaAs/AlGaAs MQW structures with heavily carbon doped wells. These results are in agreement with a detailed analysis including many-body effects for intersubband optical absorption in the valence band. The p-type MQWs were designed to have the second light hole band just above the QW barriers and with a separation between the first bound heavy hole state and the second light hole state of about 120 meV, which gives intersubband absorption at ~10 μm. Because of the much heavier effective mass of holes in the p-type structure, as compared to an n-type structure, a large reduction of the dark current is observed, which may lead to IR detector arrays operating at higher temperatures.

The structures were grown by the atmospheric pressure MOVPE process. Carbon was used as the p-type dopant. Because the growth conditions for high C doping densities and high quality AlGaAs are different, it was essential to optimize the As/Ga ratio and growth temperature to obtain a hole density of $\sim 2\times10^{19}$ cm^{-3} in the QWs and also device quality AlGaAs barriers. The MQW structures consist of 5 - 12 periods which are sandwiched between two p^+ contact layers. The well and barrier thicknesses are 56 and 300 Å, respectively. Photodetector diodes with a mesa geometry of 300×400 μm^2 were fabricated by wet etching.

The normal incidence absorption strength was measured with a FT-IR spectrometer. The absorption dependence on the polarization angle of the incident radiation was used to verify the occurrence of normal incidence absorption. The FTIR absorption peak observed at ~10 μm is in good agreement with the structural design of the MQW structures. The lineshape of the absorption spectrum with $\Delta\lambda/\lambda\sim$ 40% is similar to that obtained from bound to extended states transitions in n-type structures, which is indicative of intersubband absorption. It is found that the absorption coefficient is proportional to the doping density. For doping densities of $\sim 2\times10^{19}$ cm^{-3}, absorption coefficients of over 3×10^4 cm^{-1} for a single polarization of light are demonstrated which, for a MQW structure with 5 periods, leads to an internal quantum efficiency of ~ 16 %. The dark current is less than 10^{-9} A at 77 K for an average bias field of 33 kV/cm. These results are significantly better than what was previously attained for n-type structures. The photocurrent spectrum is characterized by a narrow peak at $\lambda \sim 12$ μm.

EFFECT OF SUBSTRATE MISORIENTATION ON THE ELECTRICAL AND OPTICAL PROPERTIES OF AlGaInP LEDs

D. V. Morgan, Y. H. Aliyu, H. Thomas and D. Lacey

Department of Electronics, School of Engineering, University of Wales College of Cardiff,

P. O. Box 917 Cardiff CF2 1XH

Visible light-emitting diodes(LEDs) are of growing interest because of their numerous potential applications, which include outdoor displays and automobile indicators. Recently quaternary AlGaInP have been investigated for optical device applications in the visible spectral region. These studies include lasers[1], and LEDs[2][3]. AlGaInP has a wide bandgap in which direct energy transitions occur in the spectral region between green and orange. This material system have exhibited high brightness LEDs ranging between red to green. It compares favourably with the best AlGaAs devices and about ten times better than the standard GaAsP:N yellow LEDs. AlGaInP LEDs enable LEDs to be used for applications that require either high output power or low power consumption.

This paper reports our investigations of the electrical and optical properties of MOCVD AlGaInP on misoriented n-GaAs substrates. Current-Voltage(I-V), Capacitance-Voltage(C-V), Deep Level Transient Spectroscopy (DLTS), Light-Current (L-I) and Spectral Response(R-S) are used characterise the LEDs. The device performances are found to be strongly dependent the substrate misorientation. The devices fabricated from substrates misoriented at 2° towards the <110> direction have about 40% light output greater than devices grown on substrates misorientation at 10° towards <110> direction, which are characterised by a shift in the peak wavelength as a result of band gap energy narrowing. The effect of the substrate misorientation are two folds namely to enhance the Zn doping efficiency and to impede the incorporation process, resulting in change of band gap energy due to a change in the atomic arrangements. The resulting consequences include the introduction of disorderliness and defect levels in the crystal.

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Resonant cavity enhanced InGaAs/AlGaAs heterojunction phototransistors with strained bulk and multiple quantum well absorbers

O. Sjölund and A. Larsson
Department of Optoelectronics and Electrical Measurements
Chalmers University of Technology
412 96 Göteborg, Sweden

Vertical integration enables dense arrays of optoelectronic elements for applications in parallel optical transmission and processing. Using vertical integration of light emitting and modulating devices, such as vertical cavity surface emitting lasers (VCSELs) and electroabsorption modulators, with detecting and amplifying devices, switching and logic functions with optical gain for fanout and loss compensation can be realized [1,2]. Devices that operate in the transmission window of the substrate are desirable since they facilitate cascading of arrays.

Photodetectors responding to wavelengths for which GaAs substrate is transparent are difficult to fabricate since lattice mismatched InGaAs has to be used as an absorber. To avoid the formation of strain induced misfit dislocations, the thickness of the absorbing layer has to be less than the critical thickness. This limits the single pass optical absorption which results in low responsivity. By placing the absorber in the base-collector depletion region of a heterojunction phototransistor (HPT) and placing the HPT in a resonant cavity one can increase the effective absorption and the generated photocurrent is internally amplified, thus the overall gain and responsivity are significantly increased[3,4]. We have studied resonant cavity enhanced InGaAs/GaAs/AlGaAs HPTs with strained bulk and multiple quantum well (MQW) absorbers.

Initially we have investigated the HPT with a bulk absorber. The HPT is similar to those reported by Ünlü et al.

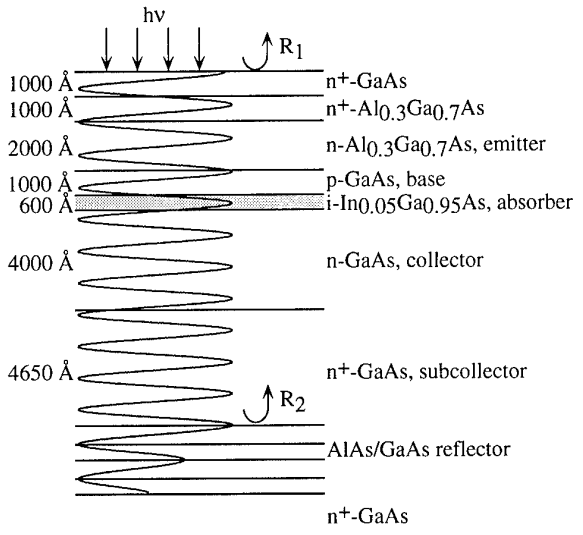

Fig. 1 Epitaxial structure for the HPT with bulk absorber along with the calculated optical field intensity for the standing wave.

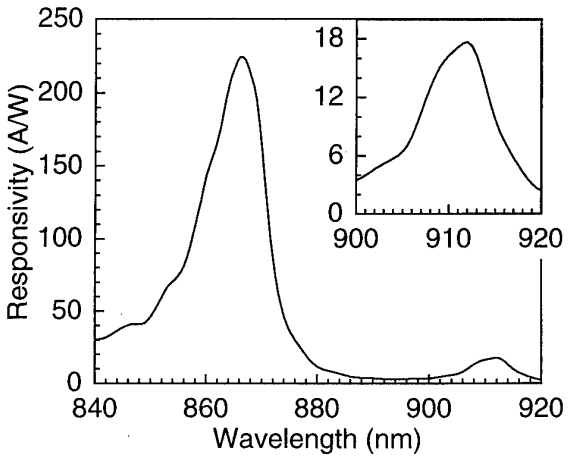

Fig. 2 Spectral response at 5V collector emitter voltage and 100 μW optical power for the HPT with bulk absorber. The inset shows an enlargement of the wavelength region of interest.

[3] and its epitaxial structure along with the intensity of the standing wave distribution of the optical field at resonance is shown in fig. 1. In this design the position of the absorber with respect to the standing wave has a large impact on the total absorption. A typical spectral response at 5V collector-emitter voltage and an incident optical power of 100 μW is shown in fig. 2 and the resonant behavior is clearly demonstrated. The inset shows the wavelength region of interest. The maximum responsivity is 18 A/W at a resonance wavelength of 912 nm. This value is lower than expected due to a somewhat lower In content than intended. The full width at half maximum (FWHM) spectral bandwidth is about 8 nm. If longer wavelengths are to be reached, more In has to be incorporated in the absorber which leads to a thinner absorber and thus lower absorption as well as a more critical matching of the absorber with respect to the standing wave.

One of the most important parameters is the uniformity of the resonant wavelength and the peak responsivity over 2-D arrays. We have measured this for HPT arrays with a bulk absorber [5]. From the uniformity measurements we conclude that the uniformity in resonance wavelength and responsivity is good within individual arrays. However, the uniformity from array to array is rather poor. Since the uniformity within an array is good, one could consider etching individual arrays in order to tune the resonance wavelength. This would, however, also modify the location of the standing wave distribution with respect to the thin absorber which will affect the responsivity.

An InGaAs/GaAs/AlGaAs RCE-HPT with maximum

responsivity at $\lambda > 920$ nm that is insensitive to the standing wave distribution is therefore highly desirable. Such a detector could be tuned to the desired resonance wavelength by controlled etching without affecting the responsivity. One method to accomplish this is to use a MQW structure as absorbing region where the quantum wells are distributed such that the integrated absorption is insensitive to the standing wave distribution. Our calculations show that this is indeed possible and that a tunability of about 30 nm is achievable.

Such an HPT has been fabricated and the initial results are very encouraging. It is designed for a resonant wavelength of 940 nm and the calculations indicate that the effect of the location of the standing wave with respect to the quantum wells on the absorption is negligible. Furthermore, if we assume that the absorption coefficient for the QWs is constant over a certain wavelength range below the excitonic resonance (in our case 925-955 nm), the total absorption at resonance is constant over this wavelength range. The nine absorbing QWs are placed in the collector region of the HPT. The structure along with the intensity of the standing wave distribution of the optical field at resonance is shown in fig. 3.

Fig. 4 shows the spectral response at 2V collector-emitter voltage and an incident optical power of 10 μW. The maximum responsivity is 52 A/W at a resonance wavelength of 931 nm. The inset shows the maximum responsivity as a function of incident optical power. As can be seen the responsivity increases dramatically with incident optical power. These results are superior to those reported earlier [4]. If integrated with a VCSEL with 2-3 mA threshold, 50 μW incident optical power on the HPT is sufficient to produce 1 mW of optical power from the VCSEL, resulting in an overall optical gain. Measurements of array uniformity are in progress.

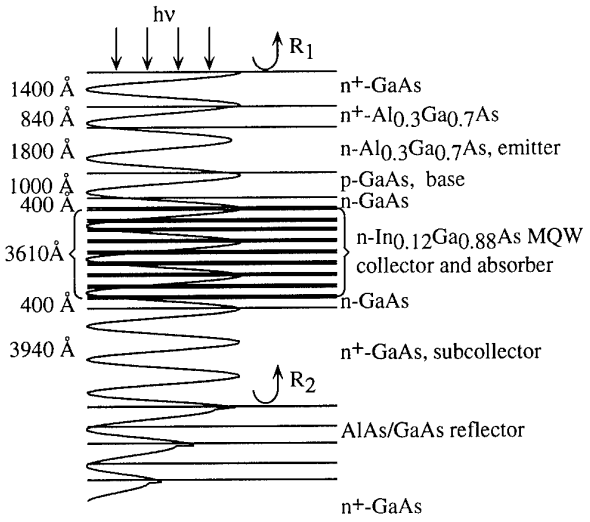

Fig. 3 Epitaxial structure for the HPT with MQW absorber along with the calculated optical field intensity for the standing wave.

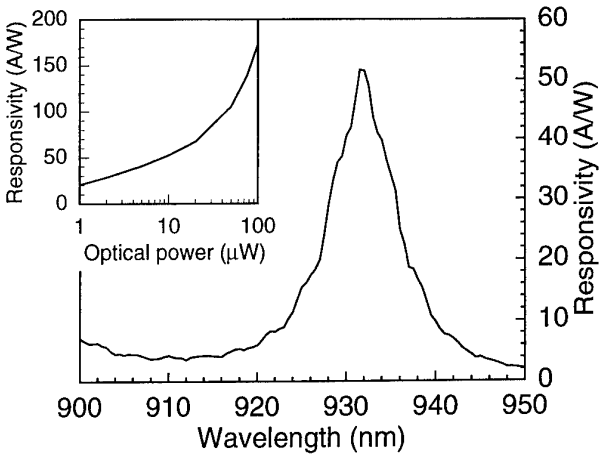

Fig. 4 Spectral response at 2V collector emitter voltage and 10 μW optical power for the HPT with MWQ absorber. The inset shows the responsivity as a function of incident optical power

In conclusion we have compared an HPT with a bulk absorber with one with a MQW absorber. In the bulk case the location of the absorbing layer with respect to the standing wave distribution is critical. Furthermore, it is difficult to reach longer wavelengths than 920 nm. In the HPT with an MQW absorber the absorption can be made independent of the location of the standing wave distribution. It can also be tuned over a large (930 - 950 nm) wavelength region with little variations in responsivity. This transistor also shows an excellent responsivity at low optical powers.

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Novel InP/GaInAs photodetector for a simple integration in HEMT circuits

M.Horstmann, M.Marso, F.Rüders, M.Hollfelder, P.Kordos and H. Lüth

Institut für Schicht- und Ionentechnik (ISI), Forschungszentrum Jülich GmbH, D-52425 Jülich

We report the first investigation of the optoelectric behaviour of an MSM-2DEG diode up to 1.3μm wavelength. The device consists of a metal-semiconductor-metal (MSM) structure above a two dimensional electron gas (2DEG) in the InP/GaInAs material system. The layer sequence is the same as for HEMT devices. Therefore our device can easily be integrated into HEMT circuits [1].

The InP/GaInAs structure was grown by MOVPE on a semiinsulating InP substrate [2]. First an undoped InP buffer layer was grown followed by a 2-DEG layer system with a strained $In_{0.8}Ga_{0.2}As$ channel, a 150nm lattice matched GaInAs which acts as a photosensitive layer, a 40nm thick InP layer and finally an n-doped GaInAs cap layer. The InP layer is used for Schottky-barrier-height enhancement [3] on GaInAs. The 80nm n-doped GaInAs cap layer is used to enhance ohmic HEMT contacts and to fabricate selfaligned MSM finger structures.

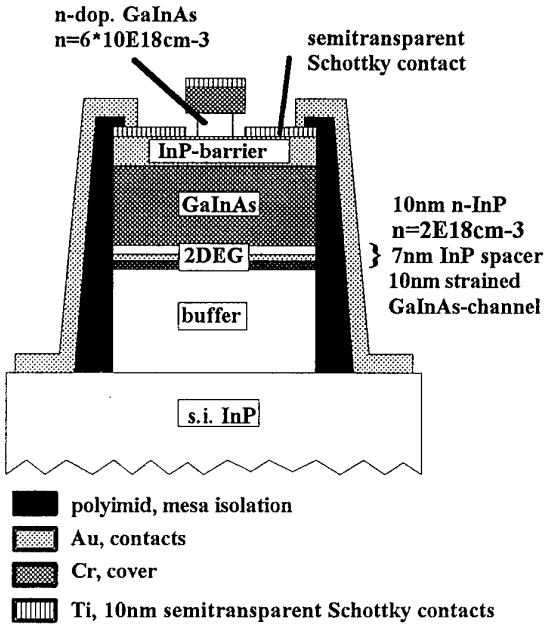

Figure 1. Cross section of MSM-2DEG photodetector

Due to the 2-DEG the electric field is mainly perpendicular to the surface and lies below the Schottky contacts. In order to prevent carrier generation in the region with low electric field between the contacts, this region is shadowed by a thick metal layer on the GaInAs cap layer. Incoming light penetrates through the 10nm Ti semitransparent Schottky contacts and generates electron and holes in the GaInAs photosensitive layer. In contrast to conventional MSM photodetectors [4], where the active length is given by the distance between the Schottky contacts, the active device length is given by the distance between the 2DEG and the semitransparent Schottky contacts [5]. This length can easily be controlled by epitaxial growth (Figure 1.).

Optoelectric measurements of a photodetector with an area of $40*25\mu m^2$ were performed by electro-optical laser sampling equipment [6] and opto-electric high frequency (rf) measurement equipment HP8510 S-Parameter test set and HP83420A lightwave test set.
The laser sampling measurements were performed by 875nm and 890nm wavelength which is the greatest available wavelength of our laser sampling equipment. Therefore the device must be cooled to 40K to prevent carrier generation in the InP layers. We found a very fast photo current pulse with FWHM of 1ps. This response was superposed by a slowly decreasing "tail" which absolute magnitude becomes smaller at higher wavelength (Figure 2.).
The optoelectric rf-measurements were performed at 1.3μm wavelength without cooling. The light was directed on the device by a glass fiber. The electric response of the device was measured by the S-parameter test set. The time behavior was calculated by fourier

transformation of the frequency domain response. We found a photocurrent pulse with FWHM of 60ps which is the resolution limit of our measurement equipment. Using windowing to surpress the effects of sidelobs caused by the fourier transform the resolution slightly enhances to 89ps FWHM. The 1.3µm sensitivity of the device is 0.19A/W (Figure 3).

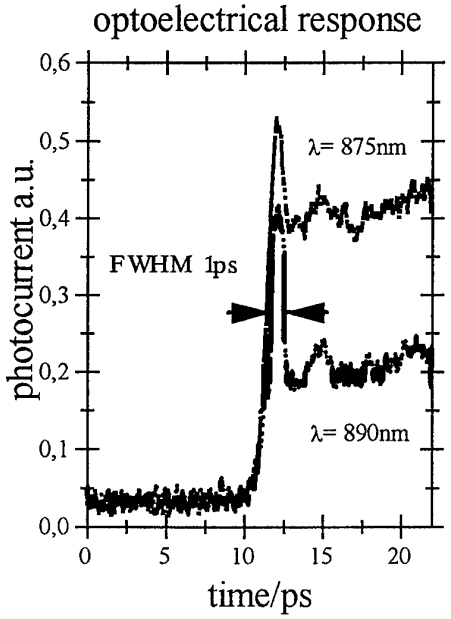

Figure 2. Optoelectrical response measured by laser sampling

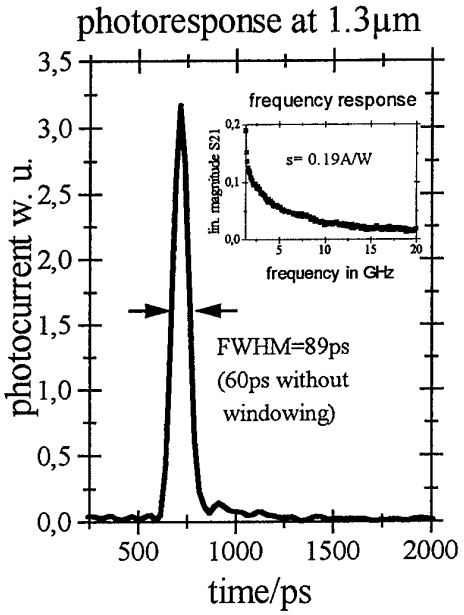

Figure 3. Optoelectrical response measured by rf-measurement equipment

The pulse measurement indicated that our device is much faster than the resolution limit of our 1.3µm measurement equipment. The "tail" observed at 890nm disappears at higher wavelength.

InP/GaInAs-HEMTs and MSM-2DEGs were fabricated on the same wafer to show compatibility to standard HEMT technology. The HEMTs have a gatelength of 1.5µm and a cutoff frequency of about 15GHz.

An integration of a MSM-2DEG photodetector with a HEMT circuit will be demonstrated. The sensitivity of photodetector will be enhanced by applying an antireflexion layer.

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NEW TYPE OF PHOTODETECTORS - INJECTION PHOTODIODES BASED ON GRADED III-V SEMICONDUCTORS

H.P. Peka, V. Radziviliuk, and A. V. Buyanov

Semiconductor Science Division, Kiev University, 252022 Kiev, UKRAINE

We have developed a new type of optoelectronic devices - long injection forward-biased photodiodes, of which the base is made from a semiconductor A_3B_5 alloy compound with a graded alloy composition (thus a graded band-gap). The unique features of nonequilibrium carrier transfer (drift in the built-in field, photon recycling) together with specific photogeneration processes in the graded-band-gap structures provide new possibilities for tunable spectral characteristics, increasing photosensitivity and decreasing influence of surface recombination, as well as for extending functional abilities of the devices.

Taking as an example GaAs-$Al_xGa_{1-x}As$ ($0<x<0.8$) long diodes, we have shown, both theoretically and experimentally, that the following features are achieved using graded-band-gap bases.

a) Spectral characteristics at T=300K can be obtained with a record selectivity (half-width of 20-35meV), where the maximum position is determined by the alloy composition of the p-n junction.

b) By using a special level of gradient compensation of the graded-band-gap base broad-band spectral characteristics can be achieved with a simultaneous increase of the current photosensitivity by 2-3 orders of magnitude in comparison with analogous homogeneous devices due to injection amplification .

c) The shape of the spectral characteristics can be conventially controlled from high-selective to broad-band by varying injection current from a low injection level to a high injection level. In the latter case the spectral range of the sensitivity covers from the lowest to the highest band-gap energy of the graded base.

d) When the band gap of the base undergoes an intervalley crossover (Γ-X crossover in $Al_xGa_{1-x}As$) a special type of spectral characteristics can be obtained as a result of a redistribution of injected carriers in the base caused by a change in electron mobility in the vicinity of the intervalley crossover.

The optimal parameters of a graded-band-gap alloy compound for each of the above-mentioned effects are calculated. The technological regimes of graded compensation are developed.

A number of complimentary methods are proposed to determine the parameters of the graded-band-gap alloy. These parameters are essential in designing injection photodiodes with controlled characteristics, such as a built-in quasielectric field, diffusion and diffusion-drift effective lengths, surface recombination rate.

SESSION 4

NOVEL STRUCTURES AND CONCEPTS

Potentials of SiGe Heterobipolar and Heterofieldeffect Transistors

A. Gruhle and U. König
Daimler Benz Research Center, D-89081 Ulm, Germany

Introduction

The booming market for computer and communication requires new components in the GHz range. Cellular and cordless telephones operate between 1 and 3 GHz, wireless local area networks use the 2.4 to 5.8 GHz band and traffic control envisages frequencies up to 77GHz.
SiGe heterojunction devices, which are at the point of commercial availability, will fulfill the demands for high volume and low cost circuits for the above applications. This is because SiGe devices have demonstrated very high frequency operation above 100GHz, low noise performance and low power consumption which favours their use in both microwave and digital circuits.
It was only during the recent few years that advances in the growth of strained SiGe layers made it possible to apply bandgap engineering to silicon-based devices. Besides new optical applications the ability of heterostructures to control independently electrons and holes allows to exceed the classical limits and tradeoffs of the bipolar junction transistor (BJT). The improved heterojunction bipolar version (HBT) offers high gain, a low base resistance and a fast base transit time. Annother device that takes advantage of heterojunctions is the modulation doped FET (MODFET) that separates dopants and carriers to obtain high mobilities. SiGe-based MODFETS are important because of their potential to improve existing CMOS circuits.

SiGe Heterojunction Bipolar Transistors

A silicon-based HBT can be built by using a SiGe layer as the base /1/. Compared with a BJT the base may be as thin as a few nm /2/ which helps to decrease base transit time and therefore the device cutoff frequency, which has reached 116 GHz /3/. In addition, the doping may be extremely high, above $10^{20}cm^{-3}$ which reduces the base sheet resistance. Values below 1KΩ/sq have been reported favouring very high f_{max} frequencies up to 120 GHz /4/ and low RF noise of 0.9dB at 10 GHz /5/. These results have been obtained from HBTs the layers of which had been grown by MBE without interruption, a technique that allows the necessary tight growth control of these thin layers. However, most of the HBTs were of a double-mesa type, unsuitable for large scale integration. In addition, the sensitive strained SiGe layers restrict the allowable temperature budget to values well below usual process temperatures. A different approach is to start from an existing bipolar transitor process and change only a few steps in order to fabricate SiGe HBTs. Base doping and Ge content have to be limited to prevent relaxation and outdiffusion. Despite these restrictions the devices reached an f_T of 113 GHz /6/. A future production technology for optimum SiGe HBTs should therefore have a low temperature budget and at the same time provide a high quality passivation, e.g. a thermal oxide to reduce 1/f noise /7/.
One application of SiGe HBTs are digital integrated circuits, which will profit from high f_T and low R_B values. A19ps fast ringoscillator /8/ and a 1GHz 12bit DAC /9/ have been reported. Most important for HBTs are microwave applications due to the high f_{max} frequency and at the same time low noise. Recently realized MMICs include a DC-15 GHz gain block with 9dB gain /10/ and a 24-26 GHz VCO.

SiGe Heterojunction Field Effect Transistors

The introduction of heterostructures provides several advantages for FETs. In a MODFET the carriers are confined in a quantum well separated from the dopant atoms leading to reduced Coulomb scattering and increased mobility. In addition, there is evidence for a velocity overshoot /11/ due to the strain in the channel layers. Finally, most important for hetero-MOSFETs is the elimination of interface scattering because of the more perfect Si/SiGe interfaces.
In the case of **n-channel MODFETs** a strained Si layer is grown on a relaxed SiGe buffer. The strain will lower the conduction band of the silicon which can be used to form a quantum well for electrons. Advances in the growth of step-graded relaxed buffers have led to record electron mobilities of 2000 cm^2/Vs at room temperature and up to 500000 at 4K /12/ which demonstrates the absence of Coulomb

scattering. MODFETs reached 340mS/mm at R.T. and 670mS/mm at 77K despite a decent gate length of 1.2µm /13/.

The mobility enhancement in SiGe-channel **p-MODFETs** is less pronounced due to intersubband and alloy scattering although theory predicts an improvement over silicon /14/. For moderate Ge-contents of around 25% the experimental R.T. mobility reached 220cm^2/Vs /15/, hardly an improvement over the value of 150 cm^2/Vs found in p-Si MOSFETs. The maximum reported p-MODFET transconductance was 167mS/mm /16/. Much more interesting are channels of pure Ge, the semiconductor with the highest known hole mobility. The necessary relaxed buffers with a high Ge percentage, however, may cause compatibility problems when combined with n-MODFET technology. In Ge channels a R.T. mobility of 1300cm^2/Vs has been reported /17/. Very promising are SiGe channels with about 70% of Ge, where R.T. mobilities of 900 cm^2/Vs have been measured /12/.

Most of the reported heterojunction MODFETs had Schottky gates.The onset of forward biasing of the Schottky diode, however, limits the useful voltage swing. The introduction of SiO_2 as an insulator surmounts these limitations. On the other hand, a high quality oxide requires Si to be at the semiconductor interface which limits the possible combinations of Si/SiGe heterostructures. These **hetero-MOSFETs** will only show the mentioned high mobilities if the carriers are kept away from the SiO_2/Si-interface where surface scattering limits the performance of normal MOSFETs. The formation of possible parasitic surface channels /15/ should therefore be avoided. SiGe hetero-MOSFETs may be used to boost the performance of CMOS circuits because of their compatible device technologies (with the exception of a lower thermal budget for SiGe devices). Particularly interesting are the p-channel devices which are typically 2 to 3 times larger in CMOS circuits than their n-channel counterparts because of the lower hole mobility. A p-MOS device with a threefold mobility would therefore result in equally sized p- and n-devices thereby significantly reducing CMOS circuit area. A possible implementation of complementary MODFETs consists of growing the layer sequences of p- and n-MODFETs on top of each other without growth interruption /18/. An adequate design of thickness, Ge composition and doping of the layers will lead to a device that can be turned into an n-MODFET or a p-MODFET only by varying the gate voltage. No channel implants and only a single poly-gate will be needed thereby reducing fabrication complexity.

Conclusion

The growth of Si/SiGe heterostructures has reached a mature level and fabrication technology of high performance SiGe HBTs is well advanced. First commercial devices and circuits will soon be available. The compatibility with existing silicon technologies assures low price and high volume production. In particular, the SiGe HBT with its high speed and low noise favours analogue microwave applications and fast digital interfaces for optical fibers.

Although the SiGe MODFET is less advanced, its potentials to boost the performance of digital, low power CMOS circuits with its huge market are considerable.

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NOVEL SUPERLATTICE LIMITER DIODES

D G Hayes, A W Higgs, D D Besgrove, D C Herbert, P J Wilding,
G W Smith and K P Hilton

DRA Malvern, St Andrews Road, Malvern, Worcs, WR14 3PS, UK

We report on the performance of novel superlattice-based microwave limiter diodes at frequencies up to 18GHz. The GaAs/AlGaAs superlattice structures were grown by MBE and fabricated into diodes using air-bridge technology in planar geometry. The symmetric dc current-voltage characteristics follow an ohmic behaviour close to the origin, but exhibit one or more plateaux with increasing magnitude of applied bias, due to the underlying negative-differential velocity of the superlattice miniband transport. The voltage width of the current plateau in each structure is determined by the length of the superlattice region.

Devices also exhibit a non-linear (limiting) behaviour in the microwave power transfer characteristics which can be quantitatively related to the diode dc current-voltage curve. Microwave measurements are made with the diodes mounted in series with a 50Ω load in a non-optimised microstrip circuit and are operated under CW and short pulsed conditions. Power limiting has been observed in a range of diode sizes at frequencies up to 18GHz. A 4x4mm^2 diode has shown 16dB isolation (*ie*, 16dB added loss when limiting) at 10GHz for an input power of 310mW. Devices have been fabricated which show limiting up to input powers of 0.5W in CW operation and 1-2W in pulsed mode.

The superlattice limiter diode is a promising novel protection device, but present devices suffer from premature breakdown and relatively high insertion loss. These limitations are not believed to be fundamental to the structure, so future devices should have better overall performance if these areas are refined by improved fabrication and superlattice design. Development of a thick plated-up air-bridge process for reduced insertion loss and higher power handling through improved heatsinking is in progress.

EXCITON LIFETIMES IN GaN AND GaInN

C I Harris, J P Bergman, and B Monemar
Department of Physics and Measurement Technology, Linköping University,
S-581 83 Linköping, Sweden

H Amano and I Akasaki
Department of Electrical Engineering, Meijo University, Tempaku-ku, Nagoya 468,
Japan

GaN and related AlGaN and GaInN alloy systems are very promising for applications as wide bandgap LEDs and injection lasers, covering a wide spectrum from UV over the visible spectral range.[1,2] For laser applications in particular, the radiative decay rates, and the influence of Coulomb correlation on such decay rates as well as on gain spectra are very important parameters.[3,4] This has recently been demonstrated for ZnSe-based quantum well diode lasers [3], and should be equally important for future GaN lasers, considering the larger free exciton binding energy in GaN (about 25 meV)[5,6] compared to ZnSe (18 meV)[7]. Optical transient spectroscopy of the bulk material can provide important information on the radiative lifetimes. At low temperatures the photoluminescence (PL) spectrum in bulk semiconductors is typically completely dominated by bound exciton emission. At higher temperatures, such as room temperature, nonradiative processes typically dominate for the excitation densities normally employed in spectroscopy. In this work we have studied PL transients in GaN and InGaN samples (epitaxial layers) of sufficient purity that the intrinsic free exciton recombination is dominant at the lowest temperatures. We have obtained values for the free exciton lifetime in GaN at low temperatures, for the first time. In addition, we have measured the excitonic lifetime in the alloy material $Ga_{0.88}In_{0.12}N$, where the radiative lifetime due to localised excitons is obtained.

The samples used in this work were grown on optical grade polished sapphire substrates by the MOVPE technique. An initial low temperature AlN buffer layer of about 500 Å thickness is deposited, to partly accomodate the large lattice mismatch (about 14%) with the sapphire substrate. The active layers are subsequently grown at a temperature of about 1000 ^{o}C.[1,8]

Low temperature time integrated photoluminescence spectra have been measured using a 0.85 m Spex double monochromator to disperse the luminescence, which is then detected using a Hamamatsu photomultiplier optimised for the UV. The samples are mounted in a variable temperature cryostat allowing measurements in the range from 1.8 K up to room temperature. Laser excitation is provided by the deep UV

line (275 nm) of an Ar+ ion laser. Time resolved photoluminescence measurements have been carried out using a Hamamatsu synchroscan streak camera. Pulsed excitation is provided from a tunable dye laser with a DCM dye synchronously pumped using a mode-locked Ar+ ion laser, frequency doubled to UV with a $LiIO_3$ crystal. Pulse lengths of around 5ps are achieved. The resulting luminescence is dispersed through a 1/4m monochromator. The overall time resolution for the total system is approximately 20ps.

Results from temperature dependent photoluminescence (PL) transient measurements on MOCVD-grown epitaxial structures of GaN and GaInN are reported. In sufficiently pure GaN layers the free exciton PL dominates even at the lowest temperatures (2K), and the intrinsic excitonic lifetimes can be obtained. We report a value of 70 ps for the radiative lifetime of the free exciton in GaN at 2K, as obtained from the PL transient of a 3 μm buried undoped GaN layer sandwiched between AlN and GaInN. This is an interestingly low value, about 40 times lower than the corresponding value for GaAs at 2K[9], approximately consistent with the difference in the oscillator strength of the exciton transitions, and reflecting the outstanding prospects for GaN as a future laser material with potentially extremely low laser threshold current densities. Above 10 K a nonradiative process dominates in our samples, and the PL decay time decreases. Above 100 K the decay time is typically less than 20 ps. This strong nonradiative process is indeed expected in these heteroeåpitaxial samples, where the severe lattice mismatch to the substrate gives rise to a very high dislocation density even in the GaN layer. The decay time of donor bound excitons in GaN is also very short, about 50 ps at 2 K. This can be understood in the same way as the analogue situation for donors in GaAs. [10]

In contrast the PL decay time in the ternary alloy GaInN, which is dominated by localised excitons at low temperatures, is much longer, about 600 ps. Decay times for excitons bound to acceptors like Zn and Mg in GaN have also been studied, and are much longer, of the order 1 ns.

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Enhanced Mobility Piezoelectric HEMT Structures on (111)B InP Substrates

L.J. Hitchens, **P.A. Houston**, M. Hopkinson, G.J. Rees.
Department of Electronic and Electrical Engineering
The University of Sheffield
P.O. Box 600
Mappin Street
Sheffield S1 3DU, U.K.

Strain in materials grown off the normal (100) plane offers the possibility of tailoring the shape of the band structure in HEMTs using the resulting piezoelectric (PE) field. The PE field in the channel layer and the barrier layers can depress the bottom of the channel below the Fermi level enhancing the two-dimensional electron concentration. In addition the PE field can overcome the space charge field between the carriers in the channel and the ionised donors by holding the carriers away from the donors and from the edges of the channel walls, resulting in improvements in the mobility. In this work a self-consistent Poisson solver computer program has been written and used in the design of optimum PE device structures in the AlInAs/InGaAs/InP system. Structures grown by MBE showed improvements in mobility compared to published results on non-PE structures.

Both conventional (tensile strain) and inverted (compressive strain) structures were grown by solid source MBE. Figure 1 shows a modelled band structure of the tensile-strained conventional (doping above the channel) AlInAs/InGaAs/AlInAs HEMT structure grown on a (111)B InP substrate. A reduction in In composition in the channel is required to give the correct PE field direction to cancel the coulomb field in this configuration. This is not optimum for the highest mobility but the resulting wider bandgap InGaAs may be useful for improved breakdown characteristics. Figure 2 shows a similar diagram for the compressive-strained HEMT grown on (111)B InP. In this case the structure displays the higher mobilities and carrier confinement.

The electron transport properties of the structures were investigated by low-field transport measurements. Hall mobilities and carrier concentrations were measured in the dark in the temperature range 16K to 300K. The tensile-strained (47% In) HEMT structures gave typical 300K mobilities of 11250 cm^2/Vs at a sheet concentration of 3.3×10^{12} cm^{-2} (figure 3). The compressive-strained (65% In) HEMT gave typical 300K mobilities of 12500 cm^2/Vs at a sheet concentration of $3.8\times10^{12}cm^{-2}$. These values are a significant improvement over the best reported HEMT results for comparable sheet concentrations and In fractions. Our results show an enhancement of both mobility and sheet concentration (5% improvement in mobility and a 19% increase in sheet concentration) which we attribute directly to the effect of the piezoelectric field removing the electron distribution in the channel from the influence of both the well-barrier interfaces and the ionised donors and flattening the bottom of the channel. Shubnikov de Haas results shown in figure 4 confirm that there is very little parallel conduction and reveal that two subbands of the quantum well are occupied.

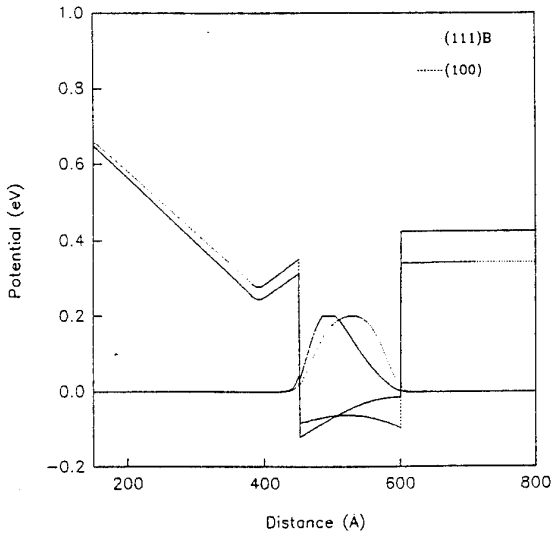

Fig. 1 Comparison of the calculated band energy for the tensile strained AlInAs/InP structure showing the shift in the electron distribution.

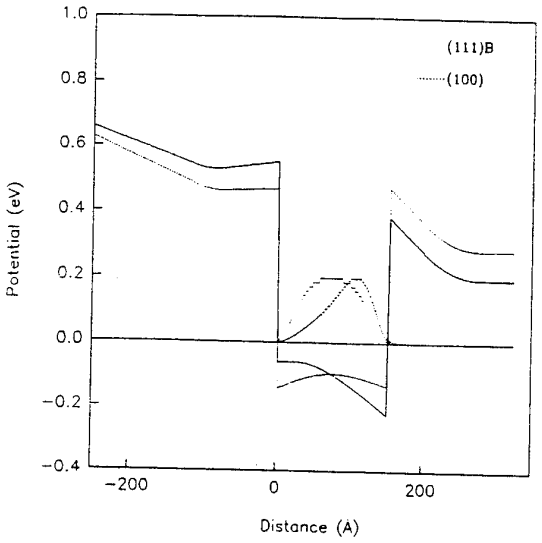

Fig. 2 Calculated band energy for the compressively strained AlInAs/InP structure

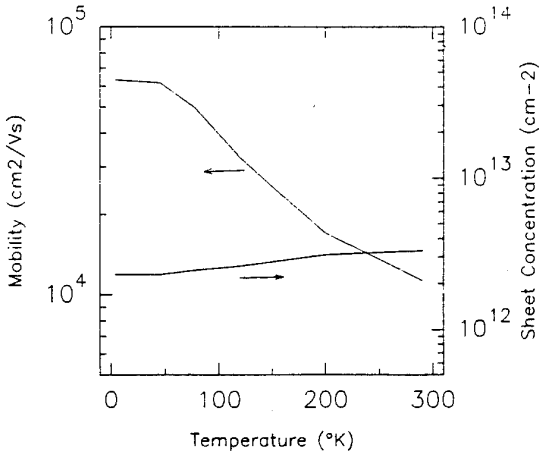

Fig. 3 Measured mobility and sheet concentration variation with temperature of the tensile strained structure.

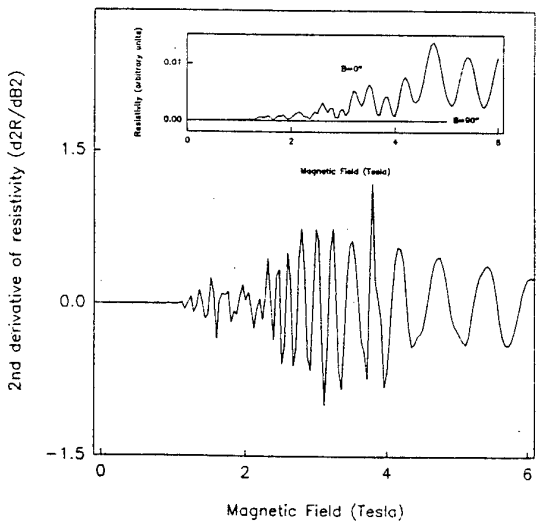

Fig. 4 Shubnikov de Haas oscillations of the tensile strained structure.

A Millimeter-wave Interferometer for Measurements of small displacements using a FECTED-VCO

A. Stelzer, A. L. Springer, C. G. Diskus, K. Lübke and H. W. Thim
Institut für Mikroelektronik, Universität Linz, Altenbergerstr. 69 A-4040 Linz, Austria
Tel.: 0043 732 2468 9300, Fax: 0043 732 2468 822

Abstract

During the last years a growing number of microwave and millimeter-wave sensors have been developed for commercial and industrial applications [1]. The main advantage of using millimeter-waves instead of optical or acoustic waves is that they are insensitive to dust, water vapour, light or high temperatures of the surrounding atmosphere. In addition, it is possible to "see through" objects which are opaque to light or acoustic waves.

In applications where distances in the range of 0.5 to 5 meters are to be measured with an accuracy of 0.2mm and below only the interferometric principle employing millimeter-waves is adequate. This principle requires an accurate measurement of the phase difference between the transmitted signal and the signal reflected from the target. However, the phase difference is unambiguous only within a distance smaller than half a wavelength of the transmitted wave. This is too small for many applications. In order to increase this range the transmitted signal must be "conditioned" in a special way. One well known methode [2] is to use two ore more frequencies but this methode requires complicated signal processing and expensive components such as analog phase shifters which are not yet commercially available above 24 GHz.

A much simpler and, to our knowledge, new solution is to use a FM-CW signal and accurately measure the interferometer output signal versus frequency. This signal containes the target position with high accuracy. There is no need for an exact linear frequency modulation of the transmitted signal, only a high accuracy in determining the frequency of the minima of the interferometer output signal is important.

The circuit diagram of our experimental set-up is shown in Fig. 1. The FM signal is fed into the transmitter horn antenna A and the signal reflected from the target is received by a second horn antenna B located close to antenna A. A small portion of the transmitter signal is guided via a 20dB directional coupler into the interferometer section consisting of a variable attenuator and a magic Tee which also receives the reflected signal. The output signals of the magic Tee contain all the information needed to calculate the position of the target. An example of such an output signal for two different positions (A and B) of the target is shown in Fig. 2.

The key element in an interferometer is the signal source capable of delivering a sufficiently large signal power. Although spectacular results have recently been obtained with pHEMTs [3] we have used a technologically much simpler and thus cheaper and yet MMIC-compatible VCO called "FECTED" or **f**ield **e**ffect **c**ontrolled **t**ransferred **e**lectron **d**evice [4] developed in our laboratory. A schematic cross-sectional view of the FECTED is shown in Fig. 4 and the monolithically integrated oscillator circuit layout is shown in Fig. 3. The frequency modulation was obtained by applying a sawtooth bias voltage to the gate of the FECTED.

With the described experimental setup it was possible to measure the displacement of a metallic target in a distance between 20 and 70 cm with an accuracy of 0.4mm. These results have been achieved without any sophisticated signal processing. Thus a precision of 0.1mm should be attainable with this method.

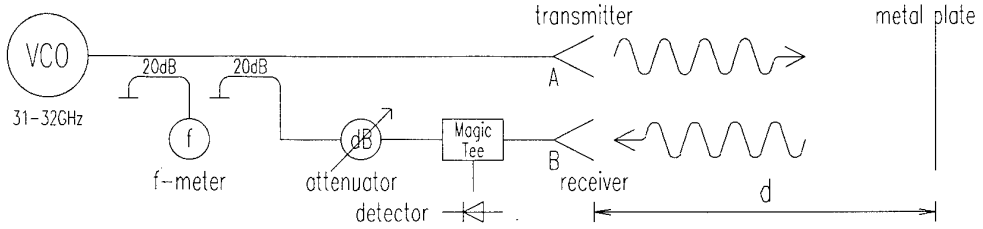

Fig.1 Circuit diagram

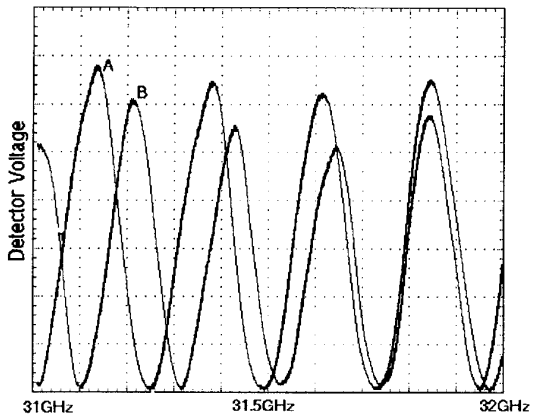

Fig. 2 Detected signal versus frequency for 2 different positions (A and B) of the target

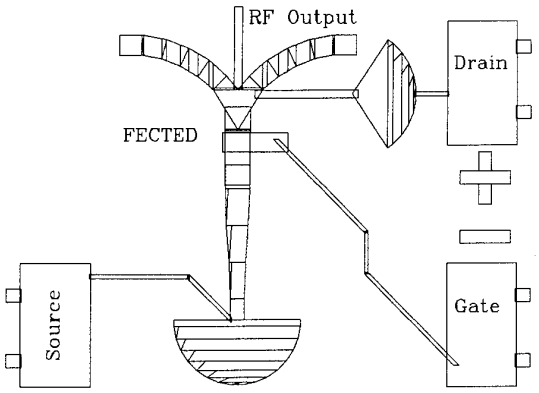

Fig. 3 Layout of the circuitry of a 33 GHz FECTED oscillator

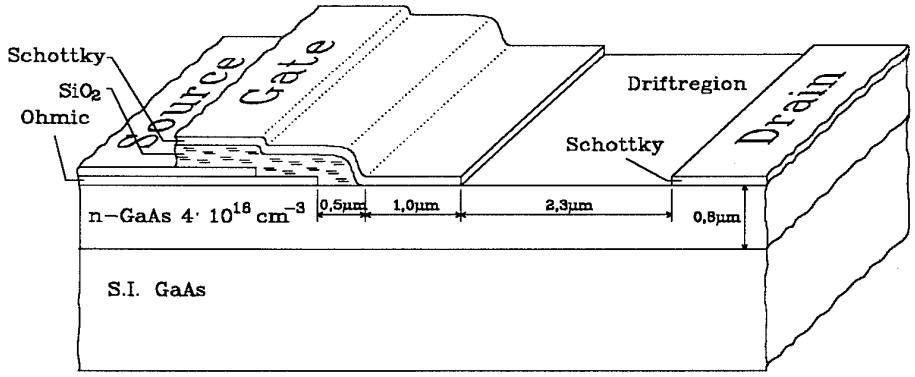

Fig.4. Cross sectional view of the FECTED

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Preparation and Characterisation of Quantum Dots of ZnSe/CdZnSe/ZnSe Grown by MBE on GaAs

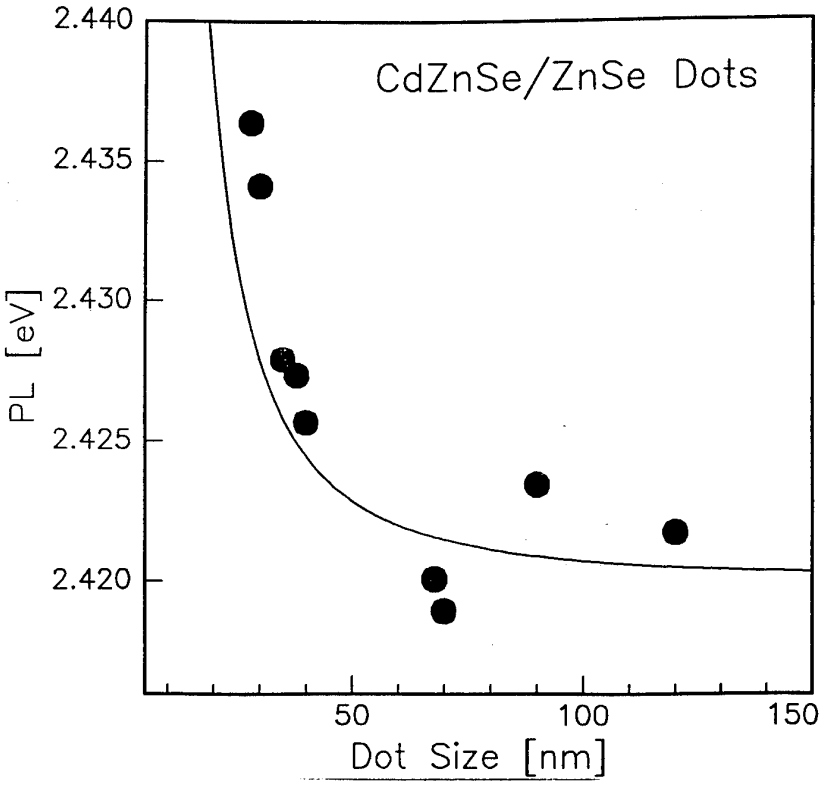
T G Andersson*, M Illing, T Kümmell, G Bacher, A Forchel, D Hommel+, B Jobst+ and G Landwehr+

Technische Physik, Universität Würzburg, Am Hubland,
D-97074 Würzburg, Germany.
*Department of Physics, Chalmers University of Technology and Göteborg University,
S-412 96 Göteborg, Sweden
+Experimentelle Physik III, Universität Würzburg, Am Hubland,
D-97074 Würzburg, Germany.

Most optoelectronic applications employ light emitted or detected by semiconductor devices operating in the near infrared (IR) or the red to green parts of the visible spectrum. Recently the interest has focused on devices operating with blue or even UV-light. Light emitting devices and detectors for short wavelengths can be expected to generate new technical applications. One striking example is the possibility to obtain high density memories in optical information processing, e.g. store much more data on a CD using short wavelengths. Two types of wide band gap semiconductor materials are available: II-VI compounds and the III-Vs based on GaN. Epitaxial layers with high crystalline perfection need to be grown on substrates giving good lattice match. The advantage of II-VI compounds over GaN is the possible lattice match with several III-V compounds which therefore can serve as substrate. ZnSe is almost lattice matched to GaAs and the CdZnSe/ZnSe system resembles some characteristics of InGaAs/GaAs, e.g. the type I band edge offset. This report is devoted to the wet chemical etching and assessment of small ZnSe/$Cd_{.2}Zn_{.8}Se$ dots when reducing the diameter from 300 to below 30 nm. When characteristic sizes are below typically 50 nm, new effects will evolve due to quantisation of electron and hole energies. The magnitude of the energy shift will depend on several parameters, primarily; effective mass, lateral size, barrier height and possibly also strain, surface effects, etc.

Epitaxial heterostructures of ZnSe/CdZnSe/ZnSe, 20/4/80 nm, were grown in a multi-chamber molecular beam epitaxy system on GaAs(001). Samples were processed by standard electron beam lithography and wet chemical etching to provide patterns of small free standing mesas. Each sample contains several arrays (100x100 μm) of different dot sizes. The etching was made to a depth of 50 to 100 nm to localise the 4 nm thick QW to the cylindrical-like top where the diameter was changed. The smallest structures therefore

constituted disc like quantum dots. Charges are confined within the band edge offset to the barrier layers and the semiconductor work function with respect to the free surface. After fabrication, the surface morphology and the lateral size of the structures were analysed by scanning electron microscopy. With the use of the 363.8 nm line of an Ar-laser and the detection with a CCD camera the photoluminescence was observed regarding change in peak position, intensity and width. All these parameters were found to alter, with reference to the 2D-layer, after reducing the dot diameters below 50 nm. The blue shift was above 15 meV due to the lateral confinement and in good agreement with calculations for a cylindrically shaped potential, cf. the figure. Reduction of the photoluminescense intensity is likely related to non-radiative recombination due to the free surfaces. Several conclusions can be drawn. One is that it is relatively straightforward to make II-VI nm-dots. Another is that the wet chemical etching does not induce optically inactive, thin "damaged" surface layers earlier reported as a result of the dry etching process.



The photoluminescence energy as a function of the measured dot size.

InAs/$Ga_{1-x}In_xSb$ Superlattices for Long-Wavelength Applications Grown on GaAs Substrates

J H Roslund, G Swensson and T G Andersson

Department of Physics
Chalmers University of Technology and
Göteborg University
S-412 96 Göteborg, Sweden

In recent years, there has been an increasing interest in applications of far-infrared radiation. In order to make this wavelength region attainable for microelectronics, a number of materials and material systems have been studied. Photonic detectors often make use of the strong interband transitions in narrow band-gap semiconductors. The most common material today for this is $Hg_{1-x}Cd_xTe$ alloys. However, the growth and processing of these materials are difficult, and interest has been focussed on the possibility of making far-infrared devices from III-V materials such as InAs and InSb and their alloys, but the wavelength limit is set to 8 μm. Therefore, to reduce the available band gap, interest has been focussed on heterostructures and superlattices. A very promising material system is the InAs/$Ga_{1-x}In_xSb$ superlattice where the low interband transition energy is due to the type II B band line-up [1]. In figure 1 can be seen the calculated cut-off wavelength, i e the maximum wavelength for a band-to-band transition, as a function of layer thickness for some InAs/$Ga_{0.8}In_{0.2}Sb$ superlattices. In this study we report growth and characterisation of a series of InAs/$Ga_{1-x}In_xSb$ superlattices.

The most obvious candidate for a substrate for this system is GaSb since its lattice parameter is intermediate to those of InAs and $Ga_{1-x}In_xSb$. GaSb is however very expensive, and it also has the drawback that it cannot be made semi-insulating. In applications, the substrate therefore has to be removed in order to discriminate the superlattice absorption from the free-carrier absorption of the substrate. In this study, we have chosen to grow the superlattices on semi-insulating GaAs substrates, which are more readily available. The disadvantage of GaAs is the large lattice mismatch, approximately 7%. Yet, we have been able to grow the superlattices with a high degree of structural quality as apparent from X-ray diffraction scans, such as the one in figure 2.

Measurement of the band gap was accomplished by measuring the carrier concentraion as a function of temperature. Since the superlattice is a narrow band-gap material, it is intrinsic at room temperature. The band gap can then be found by fitting the data to the relation

$$n \sim \exp(-\frac{E_G}{2kT}). \qquad (1)$$

We have seen good agreement between such measurements and band-gap values obtained from three-band envelope function calculations [2].

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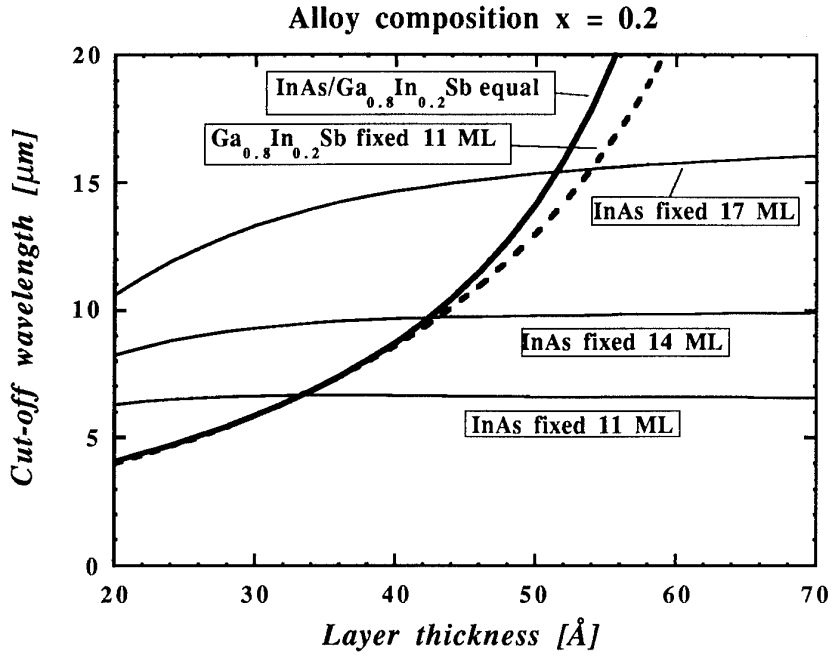

Figure 1. The maximum wavelength for band-to-band transitions in InAs/$Ga_{0.8}In_{0.2}Sb$ superlattices with one or both layer thicknesses variable.

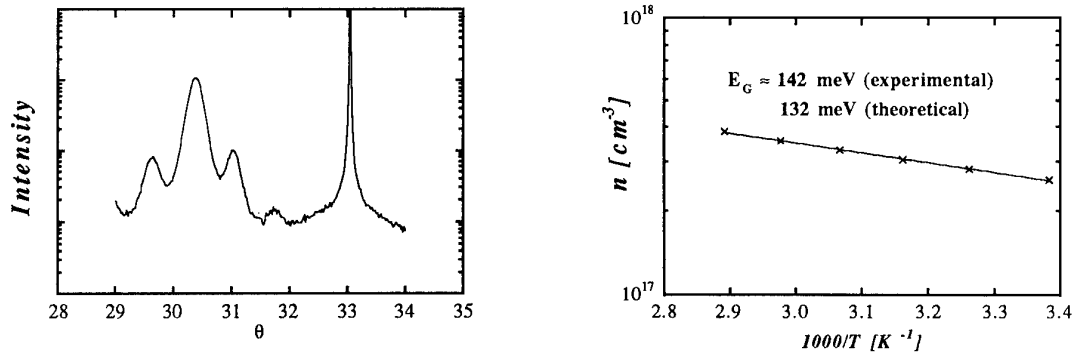

Figure 2. Experimental results from a 30-period 33 Å InAs/ 33 Å $Ga_{0.9}In_{0.1}Sb$ superlattice: an (004) high-resolution X-ray diffraction scan obtained with Cu-$K\alpha 1$ radiation (left) and carrier concentration as a function of temperature (right).

Improving the Schottky Barrier and Leakage Current of MODFETs grown on InP

Matthew Seaford*,**, Glenn Martin*, Scott Massie**, David Hartzell**, and L.F. Eastman*

* Cornell University, Department of Electrical Engineering, Ithaca, NY 14850
** Quantum Epitaxial Designs, Inc., Bethlehem, PA, 18015

Modulation doped field effect transistors (MODFETs) are currently used in both power and low noise device applications. Using solid source molecular beam epitaxy (SSMBE), it is possible to grow specific ternary compositions of indium gallium arsenide ($In_{0.53}Ga_{0.47}As$) and indium aluminum arsenide ($In_{0.52}Al_{0.48}As$) on indium phosphide (InP). When the alloy ratio in the ternary compounds result in a lattice constant different from that of InP, the structures are called pseudomorphic MODFETs (SMODFETs). It is accepted that the use of SMODFET structures where the channel layer is placed in compressive strain can be beneficial to the performance of the device.

This paper will demonstrate that the use of SMODFET structures where the InAlAs barrier layers are placed in tensile stress can be used to increase the Schottky barrier height, the maximum reverse gate bias, the conduction band offset and the channel conductance. The InAlAs barrier layers are the Schottky barrier and the spacer layer (the Atomic Planar Doped - APD layer is also present but has no thickness). For maximum channel conductance, we have previously experimentally determined 40Å to be the optimum spacer layer thickness. Using the Matthews-Blakeslee critical thickness limit for the barrier layers at 240Å, the maximum aluminum percentage is 62%. The leakage current can be calculated using the assumption of a triangular barrier for a given barrier height. The maximum reverse bias that can be applied to the gate will be defined to be the voltage when the leakage current reaches $1 mA/mm^2$.

SMODFETs with barrier layers in tensile stress can be created without detrimental effects while improving the maximum reverse gate voltage and decreasing the gate leakage current. Additionally, the conduction band offset caused by the higher aluminum percentage should allow a sheet charge of 8×10^{12} cm^{-2} in the channel of a double planar doped SMODFET. If it is found that the strained $In_{0.38}Al_{0.62}As$ results in the formation to Schottky barriers similar to those made to bulk $In_{0.38}Al_{0.62}As$, the Schottky barrier height should increase from 0.62 eV to 0.92 eV. The resulting leakage current should decrease by 10^4, while the maximum gate voltage should increase from 0.35 V to 1.05 V. If the barrier height remains at 0.62 eV, the resulting leakage current should still decrease by 10^3, while the maximum gate voltage should increase from 0.35 V to 0.85 V.

TUESDAY

SESSION 5

MODELING SIMULATION

Submitted to WOCSDICE '95

Simulation Methods for Submicron Compound Semiconductor Devices

Kazutaka Tomizawa

Meiji University, Department of Computer Science

1-1-1 Higashimita Tama-ku Kawasaki Japan

Abstract

It is known that the device simulator based on the drift-diffusion model is not applicable to the simulation of a submicron compound semiconductor device because non-stationary carrier transport becomes appreciable therein. Two methods have been used for the modeling of a submicron compound semiconductor device. One is stochastic Monte Carlo model, the other is a balance equation model. The Monte Carlo model is rather straightforward and is widely accepted as a physically based accurate model. Much has been said, however, for the validity of the balance equation model because of the difficulty in making an accurate model.

The difficulty is mainly due to the fact that the carrier transport in a compound semiconductor is usually related to the multi-conduction bands. If we try to make an accurate model, we have to deal with a large number of unknown variables: such as the carrier density, carrier momentum, and carrier energy for each conduction band. The number of variables for a balance equation model are several times larger than those employed for a drift-diffusion model. Hence, various simplified balance equation models have been developed to make the simulation possible.

We report a systematic study on various balance equation models for a compound semiconductor device by making comparative study with an ensemble Monte Carlo method. A novel explicit method which is suitable for balance equation modeling is also reported.

A Physical Description of the Behavior of GaAs MESFETs in the Deep Linear Region

Roberto Menozzi, Marco Bertoldi, Fausto Fantini, and Ged Green*
Dipartimento di Ingegneria dell'Informazione, Università di Parma
Viale delle Scienze, 43100 Parma, Italy.
*GEC-Marconi Materials Technology Limited
Caswell Towcester, Northamptonshire, NN12 8EQ, U.K.

Both linear and non-linear modeling of compound semiconductor FETs are seldom focused on the device behavior at low drain bias, since microwave applications mostly require that FETs be biased in the saturation region. However, FETs biased in the linear region have important applications, such as microwave switches and attenuators, thus physical models of the FET behavior under such bias conditions are of interest for microwave designers. In particular, a physical model for GaAs MESFETs in the resistive region must properly take into account and separate from the channel resistance (i.e. the resistance of the intrinsice device, whose effective length is in general different from the technological gate length) the contribution of source (R_S) and drain (R_D) parasitic resistances, whose dependence on the gate bias cannot be overlooked. A method to extract V_{GS}-dependent R_S and R_D at low V_{DS} was proposed in [1,2], and experimentally applied to epitaxial GaAs MESFETs in [3]; the average resistance $R = (R_S + R_D)/2$ is calculated as:

$$R = \frac{F_0}{2} - 2\left(1 - \frac{\Delta R}{F_0}\right)^{-1} F_0' \sqrt{-V_{GS} + V_{bi}} \left(\sqrt{-V_T + V_{bi}} - \sqrt{-V_{GS} + V_{bi}}\right), \quad (1)$$

where $\Delta R = R_D - R_S$ (as given by end-resistance measurements), $F_0 = lim_{V_{DS}\to 0} F$, $F_0' = lim_{V_{DS}\to 0}(dF/dV_{DS})$, $F = V_{DS}/I_{DS}$, V_T is the threshold voltage, and V_{bi} is the gate built-in voltage.

We have applied this extraction procedure to on-wafer $0.5 - \mu m$ MMIC GaAs FETs fabricated by GEC-Marconi. Although Eq. 1 was derived for constant doping devices, due to the weak dependence of the MESFET DC current behavior on the doping profile [4] we use it, without modification, for ion-implanted FETs, assuming that for our purposes the noncostant doping profile can be approximated with an effective, constant doping concentration.

Fig. 1 shows an example of the extracted average resistance versus gate bias. The behavior is consistent with those reported in [1-3], and the proper scaling with the device width is observed. Similar results have been obtained for 2-finger devices, whereas in 4-finger FETs the scaling was not obeyed, possibly due to the greater influence of the probe resistances on wider devices.

Once R_S and R_D have been extracted, the channel behavior can be modeled by means of the CGA equation (again approximating the actual doping profile with a constant concentration):

$$I_{DS} = g_0 \left\{ V_{DS}' - \frac{2}{3}(-V_T + V_{bi})^{-1/2} \left[(-V_{GS}' + V_{bi} + V_{DS}')^{3/2} - (-V_{GS}' + V_{bi})^{3/2}\right] \right\}, \quad (2)$$

where $V_{GS}' = V_{GS} - R_S I_{DS}$ and $V_{DS}' = V_{DS} - (R_S + R_D) I_{DS}$ are the intrinsic gate and drain voltages. g_0 can thus be calculated from Eq. 2 at each bias point, see Fig. 2. In the whole V_{DS} range considered (velocity saturation is expected to take place for $V_{DS} > 0.25 - 0.3\ V$ in $0.5 - \mu m$ devices) g_0 is nearly independent of V_{DS}, indicating that Eq. 2 correctly describes the intrinsic device behavior, whereas a marked dependence of g_0 on V_{GS} is seen, consistenly with [1,2], due to the reduction of the effective channel length L_{eff} with decreasing V_{GS}.

Finally, Figs. 3 and 4 show normalized values of the average resistance and of $1/g_0$ (which is proportional to L_{eff}), as a function of gate bias, for both 1- and 2-finger devices. The spread of the data is due to poor probe contact repeatability, and can be reduced by set-up improvements and by averaging results obtained on different modules. Simple, two-parameter functions have been used in the pictures to fit the data for implementation in a spice-like model.

Work is currently in progress to derive physically-based equations for $1/g_0$ and R to replace the empirical ones of Figs. 3 and 4.

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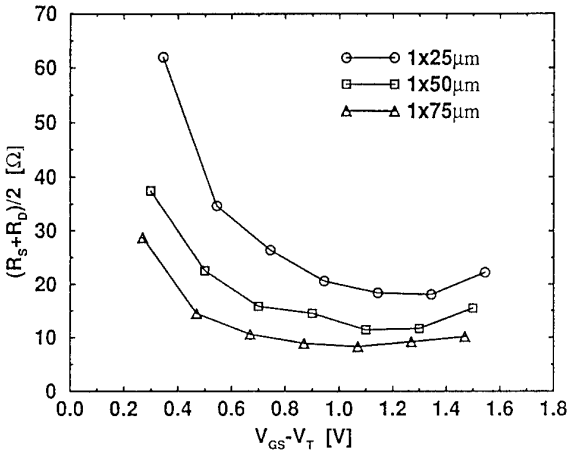

Fig. 1 Measured average parasitic resistance as a function of gate overdrive for three 1-finger devices.

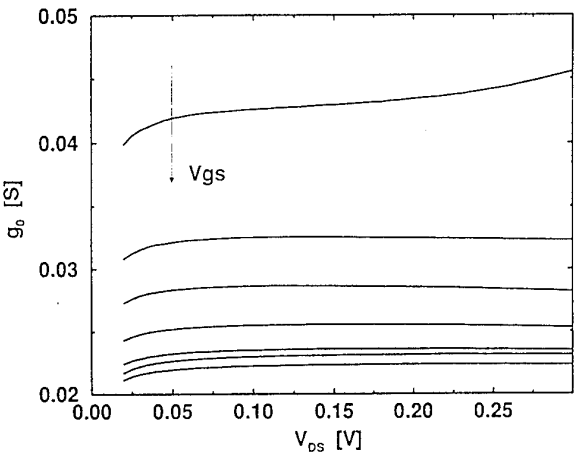

Fig. 2 Extracted channel conductance g_0 as a function of drain bias for different values of the gate voltage. g_0 is fairly constant with V_{DS}, and decreases with increasing V_{GS} due to the increase of L_{eff}.

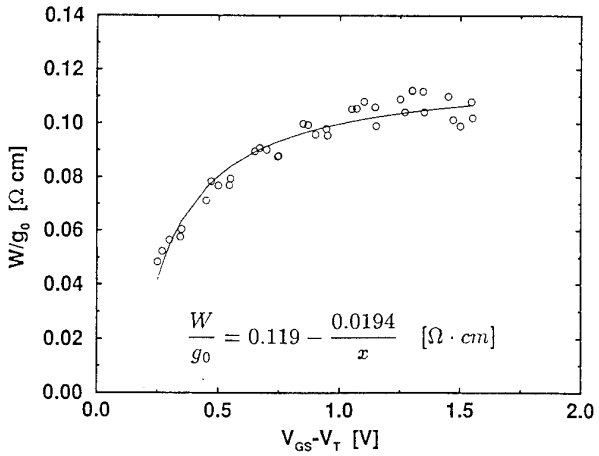

Fig. 3 Normalized channel conductance g_0 versus gate overdrive for different 1- and 2-finger devices. A simple, 2-parameter fitting function is shown (solid line).

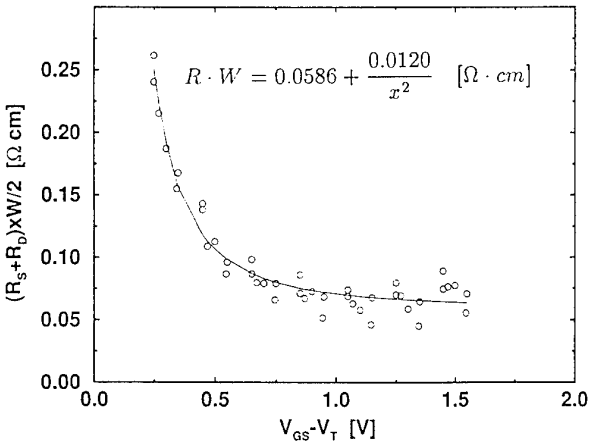

Fig. 4 Normalized average parasitic resistance versus gate overdrive for different 1- and 2-finger devices. A simple, 2-parameter fitting function is shown (solid line).

Workshop on Compound Semiconductor Devices and Integrated Circuits (WOCSDICE)
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Large-Signal Design Considerations of InP/InGaAs Heterojunction Bipolar Transistor-based OEICs

D. Pavlidis, A. Samelis, S. Chandrasekhar* and L.M. Lunardi*
Department of Electrical Engineering and Computer Science,
The University of Michigan, Ann Arbor, MI 48109-2122, USA
*AT&T Bell Laboratories, Crawford Hill Laboratory, Holmdel, NJ 07733, USA

InP/InGaAs HBTs play a major role in the development of optical receivers for long wavelength operation due to their material compatibility, high speed of operation and possibility of integration with PIN photodiodes. High bit rate Optoelectronic Integrated Circuits (OEICs) built with them are expected to have at least as good noise performance as FET-based circuits. Although significant effort has been made in developing OEICs with high sensitivity characteristics, the large signal operation of photoreceivers is not well understood. This can, however, play an important role in determining system performance. The use of an Er-doped fiber amplifiers (EDFA) before the receiver can for example, result in better receiver sensitivity but is also associated with high levels of power delivered by the PIN diode and thus large-signal operation of the HBT OEIC. This paper addresses issues of large-signal modeling of InP/InGaAs HBTs and OEICs built with them.

The InP/InGaAs HBTs had 3μm x 8μm emitters which are representative of geometries used in OEICs. Their base-collector junction area was 7μm x 20μm. The devices were characterized at DC, and high frequencies under small and large-signal operation conditions. A large-signal model suitable for InP HBTs was developed and applied to individual devices and their integrated circuits. DC parameters were extracted for this purpose from forward and reverse Gummel plots. They permitted evaluation of the saturation currents, ideality factors, base current components and resistances R_B, R_C and R_E. The model takes into account the breakdown characteristics by incorporating to the conventional Gummel Poon model a current source I_{BR} connected in parallel to the base-collector junction. An additional diode connected in parallel to a resistor R_{BR} was incorporated in the same branch to account the multiplication factor (M) of I_C. This circuit arrangement allows good simulation of the soft I_C-V_{CE} trends observed near breakdown of InP/InGaAs HBTs. Very good agreement could be obtained between experimental and modeled DC characteristics of the HBTs as shown by the results of Fig.1.

The analytical modeling techniques developed earlier for the high frequency characteristics of HBTs were applied and combined with "cold" S-parameter tests allowed accurate modeling of the intrinsic and parasitic elements. The InP/InGaAs HBTs were next characterized under large-signal conditions up to 10GHz using electromechanical tuners in an on-wafer probing configuration developed in our laboratory. Good agreement was obtained between the experimental and theoretical gain vs. input power characteristics. The incorporation of breakdown effects in the model results in good agreement with experimental results. Power saturation was found to occur at small input levels of the order of -8dBm suggesting that the HBT OEICs may exhibit large-signal operation depending on system configuration i.e. use of EDFA and circuit design.

The load-pull characteristics of the InP/InGaAs HBT are shown in Fig.2 at -18.2dBm of input power. A basic coupled buffer amplifier OEIC was designed with these devices. The frequency response of its transimpedance characteristics are shown in Fig.3 under various input power levels. The complete circuit was analyzed by incorporating the HBT model developed in this work in LIBRA and allowing therefore large-signal simulation in the frequency domain as for microwave circuits. The results demonstrate that depending on input power level the transimpedance can change leading to performance variations. To understand these effects the individual transistor performance was analyzed. It was found that their input base current was increased with input power and the changes were more important for the output HBT of the OEIC. These changes lead to a modification of S_{21} and S_{11} of the amplifier as shown in Fig.4 and thus modify the transimpedance. The importance of these effects will depend on OEIC implementation and circuit design.

Overall, the large signal characteristics of InP/InGaAs HBTs and OEICs built with them are studied and OEIC performance variations are reported under large-signal conditions.

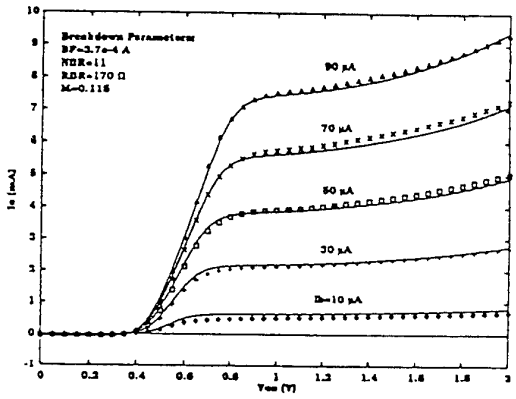

Fig.1 InP/InGaAs HBT Measured and Modeled I_{CE}-V_{CE} Characteristics

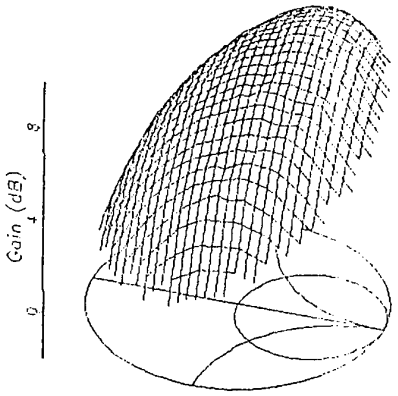

Fig.2 Load-Pull Contours of an InP/InGaAs HBT at 10GHz

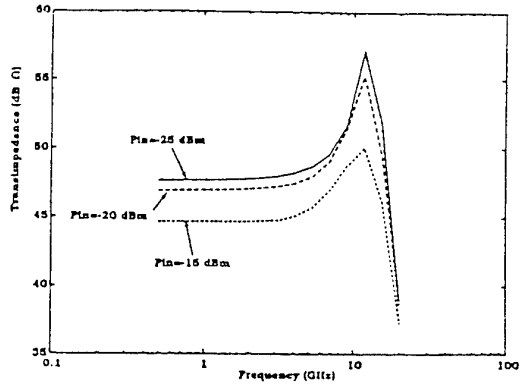

Fig.3 Transimpedance variations with input power level

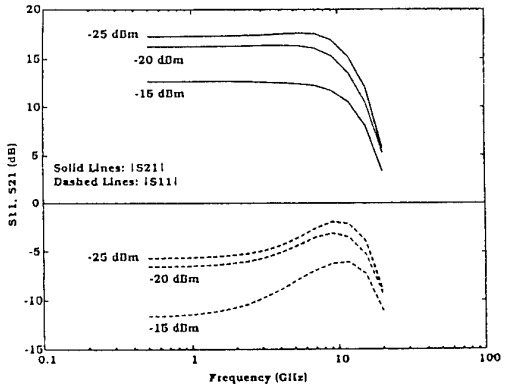

Fig. 4 S-parameter variation of amplifier OEIC with input power level

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DESIGN CONSIDERATIONS FOR LOW–NOISE APPLICATIONS OF SiGe HBTs

U. Erben and H. Schumacher

Dept. on Electron Devices and Circuits, University of Ulm, D-89069 Ulm

Recent progress in SiGe HBT development resulted in a transit frequency and a maximum frequency of oscillation of 116 GHz and 120 GHz, respectively [1]. The high base doping concentration in the range of $10^{19}\ cm^{-3}$ made possible by the base–emitter heterojunction delivers a small base resistance as well as a high current gain at small collector currents. These are necessary prerequisits for a good low–noise performance of SiGe HBTs. At 2 GHz a minimum noise figure of 0.35 dB with more then 10 dB associated gain was already observed. At a frequency of 10 GHz the minimum noise figure increases to 0.8 dB with 5.5 dB associated gain [2].

In the past the investigtions were mainly focused on the enhancement of the noise performance by device optimization. This leads to a more detailed insight into the noise and gain behaviour of SiGe HBTs. First, with conservative extrapolation of the present technologies a minimum noise figure of less than 1 dB at 20 GHz seems to be feasible [2]. Second, the gain performance at noise optimum input match is mainly determined by the collector–base feedback capacitance. A low doped collector enables an associated gain of more than 10 dB at 10 GHz [3]. However, with the enhanced noise performance the locus of the noise optimum input match moves toward an open circuit impedance.

A design study of a low–noise amplifier at 1.7 GHz for a METEOSAT front–end will exemplify additional design constrictions. The target of this design study is to investigate the feasibility of a minimum noise figure of 1 dB with 20 dB associated gain in such a 50 Ω–matched amplifier using SiGe HBTs. A hybrid microstrip circuit including two discrete SiGe HBTs is used to verify the simulation data.

Matching networks are needed to obtain a noise optimum match of both stages, as well as a transformation to the 50–Ω–output impedance. Assuming *ideal* matching networks, a minimum noise figure of 0.8 dB with more than 20 dB gain were predicted from the simulation. Unfortunately, *real* matching networks are lossy and degrade the noise performance of the amplifier. This results in a noise figure of 2.3 dB with 19 dB gain [4]. Consequently, conventional matching techniques were unsuitable for the intended purpose.

In general, there are two approches to overcome the problems mentioned above, a circuit related and a device related one.

First, the passive matching networks have to be substituted using an active matching technique. In principle, the input impedance and hence the noise optimum input match of an SiGe HBT in common–base configuration is at several bias conditions near 50 Ω. This principal behaviour was

already proven on multi–finger SiGe HBTs. Simulations have shown that the biasing resistor at the emitter node, which is in parallel to the input port, contributes additional noise to the amplifier. High supply voltages were needed to increase this resistance in order to minimize the noise figure to values below 1 dB at 0.9 GHz.

Second, based on theoretical investigations a significant correlation between the noise performance, the noise optimum input match and the dynamic input resistance was observed. Especially at frequencies below 5 GHz, the minimum noise figure decreases with increasing current gain [2]. However, with increasing current gain the dynamic input resistance in common–emitter configuration increases and the magnitude of the noise optimum input match $|\Gamma_{opt}|$ moves towards one. While small minimum noise figures are desirable, the magnitude of Γ_{opt} can be lowered only by increasing the collector current. On the other hand, an increasing current tends to increase the noise figure. The introduction of multi–finger devices in the first stage can solve this problem. The greater emitter area shifts the current, where the minimum noise figure occurs, to higher current levels. Additionally, the noise figure benefits from the drastically decreased base resistance, which now contributes much lower thermal noise. The simulations of a two–stage low–noise amplifier including a multi–finger HBT in the first stage predicts a minimum noise figure of 0.8 dB with 18 dB gain well up to frequencies of 2.4 GHz.

Especially, the high transformation loss in the input matching network of the first stage limits the noise performance of an conventionally designed low–noise amplifier. Noise–figure demands of state–of–the art amlifiers can only be met by simultaneous optimization of transistor and circuit structure. Matched low–noise amplifiers with multi–finger SiGe HBTs as the first stage common–emitter configuration can deliver small noise figures of less than 1 dB up to frequencies of 2.4 GHz.

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On the Influence of the Interface States on HBTs.

J. Grajal, V. Krozer*, H.L. Hartnagel*, J. Gismero.

ETSI. Telecomunicación. Polytechnical University of Madrid, Ciudad Universitaria s/n, 28040 Madrid, Spain. Phone: 34-1-3367358. Fax: 34-1-3367362.

* *Institut für Hochfrequenztechnik, Technische Hochshule Darmstadt, Merckstr. 25, D-6100 Darmstadt, Germany. Phone: 49-6151-162162. Fax: 49-6151-164367*

A semiconductor interface is described primarily by the discontinuity in the conduction band ΔW_c, which is created by the shift of the band structure of the materials at the heterojunction, and by localized states at the interface [1].

The interface states are basically due to the disarrangements of the ideal periodic lattice and the contamination of the interface. The interface states give rise to positive and negative electric charges in the immediate vicinity of the interface in a finite but thin region. For simulation purpose, the interface is modelled as an ideal two-dimensional surface and the charge distributions in the interface layer degenerate to surface charge densities and surface dipole densities. The surface dipole densities are caused by the difference in the gravity centers of the positive and negative charges and cause a discontinuity of the potential at the interface.

Therefore, the electrostatic properties of the interface can be characterized by the conduction band discontinuity ΔW_c, which absorbs the interface dipole density effect, and the surface charge density σ. The interface conditions for the Poisson equation (x axis is the normal direction to the interface) are then:

$$-q(\varphi_2-\varphi_1) = \chi_2-\chi_1+\Delta W_c$$

$$\varepsilon_2\frac{d\varphi_2}{dx} - \varepsilon_1\frac{d\varphi_1}{dx} = -\sigma$$

Table I. HBT Structure for simulation.

HBT-Structure	Material	Doping(cm^{-3})	Length(nm)
Emitter-C	GaAs	1e18	100
Emitter-1	GaAs	4e17	350
Emitter-2	AlGaAs(0-.42)	4e17	20
Emitter-3	$Al_{.42}GaAs$	4e17	30
Base	GaAs	2e19	120
Collector	GaAs	4e16	650
Subcollector	GaAs	1e18	100

These conditions have been used in a one-dimensional simulator for HBTs, which includes thermionic-field emission at the interface [2]. The HBT structure used for the simulations is summarized in Table I. Figure 1 presents the band diagram of this HBT with $V_{be}=V_{cc}=1.0V.$, no interface charge is taken into account. The transport through the barrier is dominated by thermionic-field

emission. If a surface charge density of $\sigma=10^{-6}$ C/cm^2 is supposed, the barrier is lowered and the thermionic-field emission process do not limit the carrier injection, Figure 2. It has been assumed in the last two examples that there is no surface dipole density.

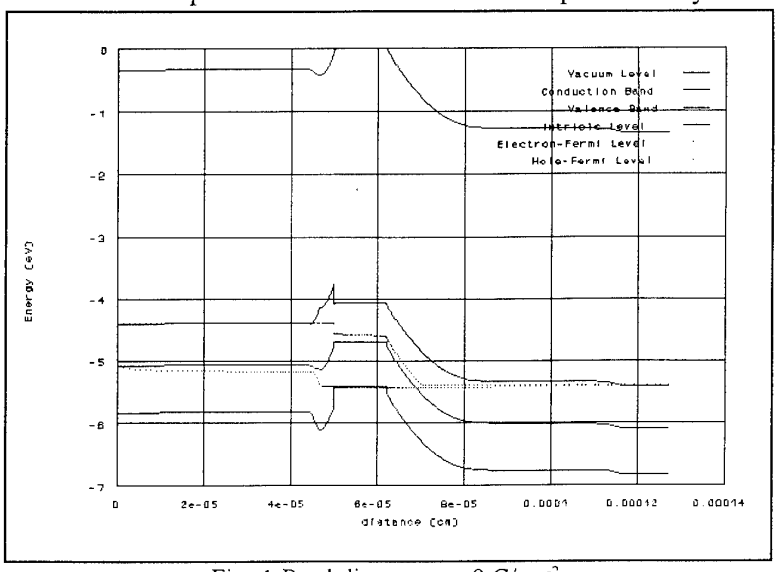

Fig. 1 Band diagram. $\sigma=0$ C/cm^{-2}

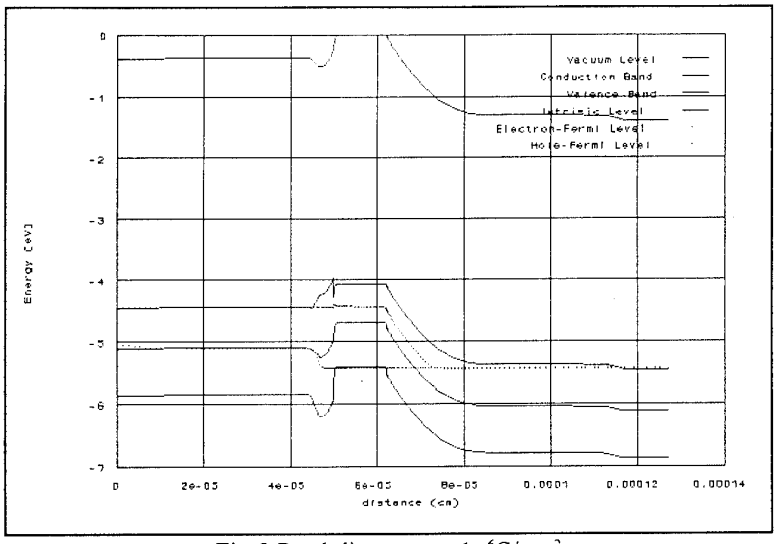

Fig.2 Band diagram $\sigma=1e^{-6}$C/cm^{-2}

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AlGaN/GaN MODFET Performance

Lester F. Eastman, J. Burm, and W.J. Schaff
School of Electrical Engineering and National Nanofabrication Facility, Cornell University, Phillips Hall
Ithaca, New York 14853-5401 USA

A simple analytical method will be presented to cover the design optimization of the 2DEG in AlGaN/InGaN/GaN MOSFET's. The analytical results will be compared with those for optimized MODFET structures on GaAs and InP. Using an empirical scaling of mobility vs doping ion density, the limiting mobility values for Zinc Blende (4,000 cm^2/V-s) and Wurzite (2,000 cm^2/V-S) are predicted. Initial experiments on AlGaN/GaN Wurzite* MODFET's will be presented, showing $f_t \geq 20$ GHz and $f_{max} \geq 75$ GHz at 20 V drain bias with .25 μm gate length. The frequency response rises monotonically with drain bias voltage, leading to speculation regarding especially high electron velocity at high electric fields. The device characteristics at operating temperatures up to 300°C will be presented, showing that the proton bombardment isolation is not effective at high temperature. With improved ohmic contacts, improved channel sheet conductance, and with thin planar-doped barriers, it is expected that f_t values over 100 GHz and f_{max} values over 200 GHz will be obtained at high power levels.

* Materials supplied by A.Khan of APA Optics, Minneapolis, MN.

WOCSDICE 95

CAPACITANCE MODEL FOR DOUBLE BARRIER RESONANT TUNNELING DIODES

T.G. van de Roer, H.C. Heyker, M. Kwaspen, M. Lepsa, W. van der Vleuten,
Eindhoven University of Technology, Department of Electrical Engineering,
P.O. Box 513-EEA, NL-5600 MB Eindhoven, The Netherlands.
tel. +31.40.475106, fax +31.40.448375, E-mail: t.g.v.d.roer@ele.tue.nl

SUMMARY
A model for the capacitance of Double Barrier Resonant Tunneling diodes has been made taking account of the finite residence time of electrons in the quantum well. Microwave impedance measurements in the frequency range 0.45-18 GHz on $Al_{0.4}Ga_{0.6}As$/GaAs DBRT's (device #1, see Fig. 1)) have been reported previously [2]. The capacitance shows a peak in the negative conductance region preceded by a dip. A second device (#2), made on semi-insulating subtrate with a layout designed for a microwave wafer prober, has been characterised to 40 GHz. The barriers are now made of pure AlAs and are only 2.5 nm thick. As a function of bias voltage the low-frequency of this device shows the same behaviour as device #1. Because of the greater frequency range we now see a stronger frequency dependence of the conductance and capacitance.

The equivalent circuit is based on the following considerations:

- there is accumulation of negative charge in the accumulation region and in the quantum well between the two barriers, and positive charge in the depletion region. These are represented by three capacitances.
- there is accumulation of negative charge in the accumulation region and in the quantum well between the two barriers, and positive charge in the depletion region, the total charge being zero.
- electrons are transported between these layers by tunneling, a process that is represented by two current sources, see Fig. 2.
  At d.c. these sources are equal because of current continuity. At higher frequencies we represent the time-dependence by a delay of I_2 with respect to I_1: $I_2(t) = I_1(t-\tau)$ where τ is the average time the electrons spend in the quantum well.
- the device voltage is split into two parts as shown in Fig. 1. Since the tunneling current depends on both voltages, the current sources must be functions of both V_1 and V_2.

At d.c. these functions are identical because of current continuity. At higher frequencies however this cannot be true anymore. Since a full time-dependent solution of Schrödinger's equation is not available at this time, we represent the time-dependence by a delay of I_2 with respect to I_1: $I_2(t) = I_1(t-\tau)$ where τ is the average time the electrons spend in the quantum well. In the small-signal equivalent circuit this means that we can write the current sources as $I_1 = g_1V_1 + g_2V_2$, $I_2 = I_1\exp(-j\omega\tau)$.

The parameters of the equivalent circuit are obtained from a previously developed d.c. model [2] that accurately describes the I-V characteristic and the charge distribution in a DBRT.

The calculated capacitance of device #1 is plotted together with the one extracted from the microwave measurements reported in (3) in Fig. 3. Apart from an offset the agreement is quite good.

The results on device #2 are shown in Fig. 4, where the capacitance extracted from on-wafer measurements is compared to calculations. Evidently the model also explains the frequency dependence, apart from an offset which could be due to parasitics.

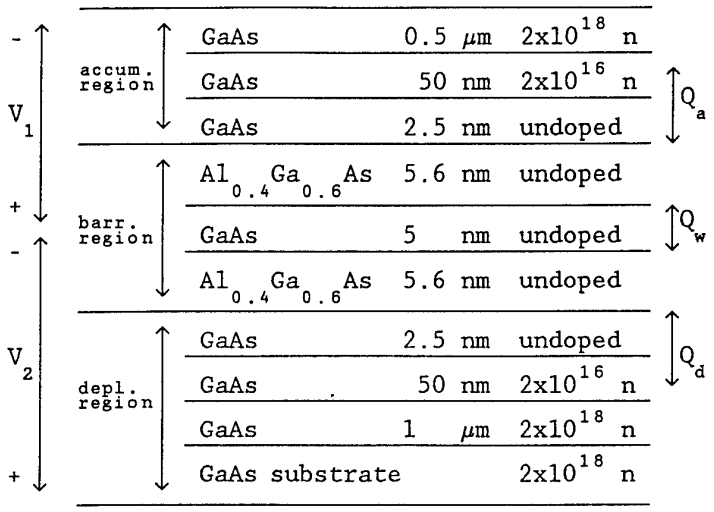

Fig.1.Device layer structure.

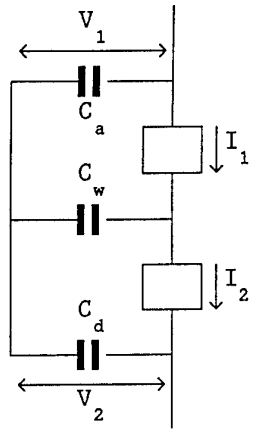

Fig. 2. Equivalent circuit

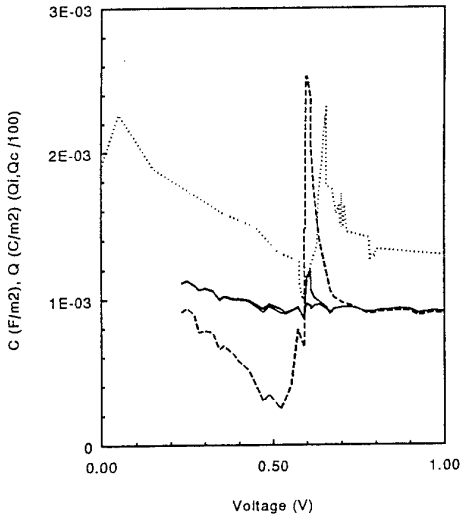

Fig. 3. Capacitance vs. bias for device #1.
.....measured
--------present model
————quantum C model

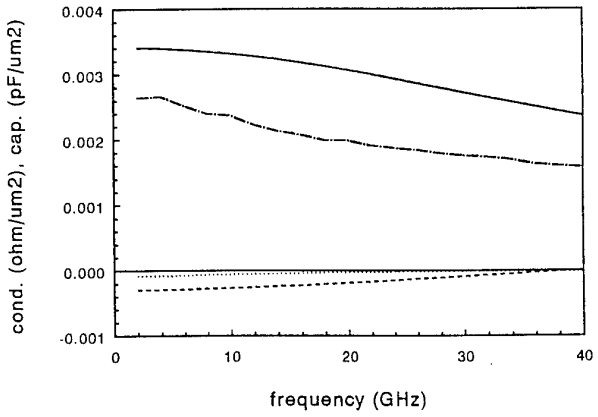

Fig. 4. Conductance and capacitance vs. freq., device #2.
-.-.-.-C meas. ————C model
.....G meas. - - - -G model

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New MODFET Equivalent Circuit Model: Extraction and Validation to 120 GHz.

P. J. Tasker

Fraunhofer Institut für Angewandte Festkörperphysik (IAF), Tullastraße 72, 79108 Freiburg, Germany.
Tel. +49 761 5159 561 Fax. +49 761 5159 565 e-mail: tasker@iaf.fhg.de

Abstract

A new MODFET circuit model has been developed, since it was found that to accurately simulate measurement data above 75 GHz the conventional MODFET circuit model must be modified. This new model accounts for distributed effects in the transistor layout and includes a modified intrinsic transistor circuit topology. It has been experimentally validated by on-wafer S-parameter measurements performed to 120 GHz.

Introduction

In the development of millimeter-wave MMICs, cost reduction is a critical issue. Low development costs require MMIC performance to meet specifications at the first pass which can only be achieved if an accurate CAD design data base is available. For the active device, the MODFET, this requires the use in CAD tools of a scalable small signal equivalent circuit model that will accurately simulate the transistor S-parameters as a function of gate width. This model is generally determined from S-parameter measurements performed below 65 GHz while the frequencies of interest for future MMIC applications are above 75 GHz. Design of these MMICs, therefore involves simulating the transistor performance by extrapolating beyond the measurement bandwidth. The validity of this extrapolation and hence the circuit models has, to date, not been directly tested with S-parameter measurements at the frequencies of interest (> 75 GHz).

Circuit Model Extraction and Validation to 120 GHz

The circuit model element values are generally extracted from an appropriate sequence of measurements performed on both the active transistor and "test" structures. The scalable circuit model commonly used containing an active (intrinsic) Y-matrix, in series with a parasitic Z-matrix, in parallel with a parasitic Y-matrix (figure 1) and thus involves the extraction of 17 element values. *A "rule of thumb" for independent extraction of these element values is that each shell requires a unique set of measurements:* "open" test structures, "Cold" FET Forward bias and active bias point measurements. It was found previously that the models extracted using this procedure could provide a very good fit to the measured S-parameters up to 75 GHz and were successfully used in the design of MMIC operating up to 80 GHz [1,2].

In order to have a good fit to the measured S-parameters up to 120 GHz, however, it was found that the model topology must be modified, as shown in figure 2. First the parasitic Y- and Z-parameters have to be distributed between four shells. This modification is required in order to account for the distributive effects associated with the finite dimensions of the transistor layout. Secondly the intrinsic output capacitance c_{ds} must be located outside the parasitic resistances r_d, r_s. This modification indicates that the extrinsic fringing electric fields between the drain and source metalizations are the dominant contribution to the output capacitance. Figure 3 shows the excellent agreement that can be achieved between the measured S-parameters and the modeled S-parameters using the new scalable extracted circuit model for a 100 x 0.15 μm^2 PMODFET. This excellent agreement is only achieved if the distributed parasitic circuit topology and the extracted intrinsic circuit model shown in figure 2 are used.

It is important to note that in this work the increased bandwidth was used only to optimize the circuit topology, the number of independent extracted element values remained constant. The more complex circuit must still be extracted using the previously described procedure, since the extracted parasitic element values were found to be frequency independent to 120 GHz. Increasing the number of independent circuit elements to be extracted would require the introduction of additional "test" structures.

Conclusion

A simple physically valid MODFET circuit model has been developed, for the first time, that can model correctly the measured S-parameters to 120 GHz. The development of this model involved the formulation of parameter extraction techniques and determination of the correct model circuit topology. For model verification broad band on-wafer S-parameter measurement systems covering the frequency band from 45 MHz to 120 GHz were developed.

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Acknowledgments

The author would like to thank the all the members of the processing group at the Fraunhofer Institute who fabricated all the transistors and MMICs used in this work. This work was supported by the BMVg and BMFT.

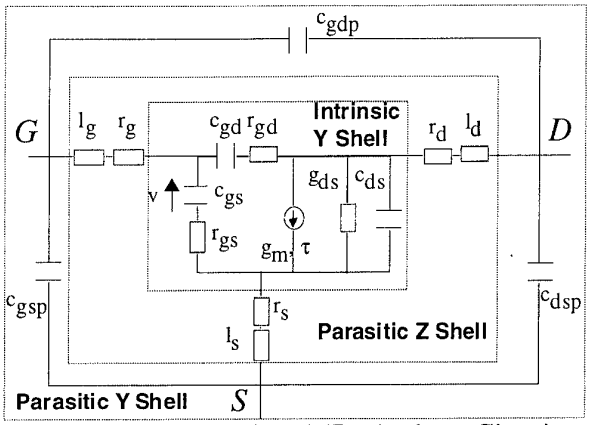

Figure 1. Small Signal Equivalent Circuit Model commonly used for modelling MODFETs formulated from series and parallel connections of simple Y- and Z-matrix two port circuits. The number of circuit model element values are 17.

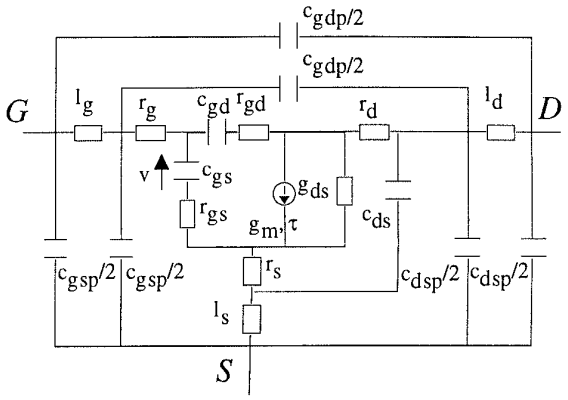

Figure 2. Small Signal Equivalent Circuit Model required for modelling MODFETs to 120 GHz. The parastics are distributed and the output capacitance is relocated. However, the number of circuit model element values is still 17.

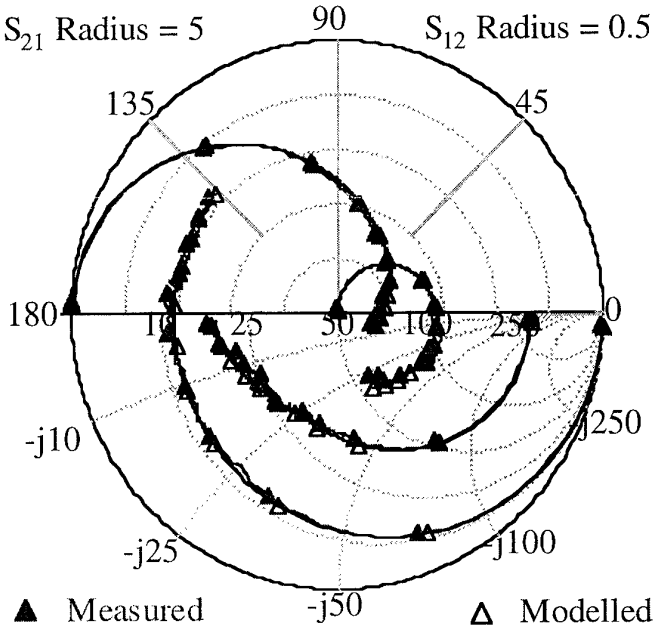

Figure 3. Comparision between measured and modelled S-parameters of a 0.15 x 100 μm^2 MODFET biased for low noise (V_{ds}=2.5 V I_{ds}=100 mA/mm) from **0.5 GHz to 118.5 GHz**.

SESSION 6

TRANSISTORS I

Microwave HBT Power Devices and Applications

(Invited Paper)

Burhan Bayraktaroglu
Westinghouse Electric Corporation
Advanced Technology Laboratory
P.O. Box 1521, MS 3K13
Baltimore, MD 21203
Tel: (410)765-2947
e-mail: burhan.b%wec@dialcom.tymnet.com

The HBT technology is rapidly maturing. Many of its promising technological advantages have been turned into reality in microwave circuit applications. While the advances in the basic device technology will continue to provide opportunities for new applications, the level of maturity achieved now can provide an accurate assessment of the impact of this technology for present and future systems. The level of maturity is also sufficient to allow an assessment of basic technological limitations.

The application of HBT in power amplifier circuits can be closely correlated to its intrinsic strengths in power density, linearity, high voltage, and low-Q output impedance. The major application areas are: a) high power and efficient amplifiers, b) linear amplifiers, and c) wideband amplifiers. The high voltage capability aids both linearity and power output capability.

In **power amplifier** applications, the high intrinsic power density provides the means to achieve the compactness necessary for efficient implementation of monolithic circuit techniques. Such amplifiers have been fabricated for personal communication applications at L/S-bands[1,2] and for military applications at X-band[3]. Although this technology is making progress toward the mm-wave frequencies, at present, the major applications are below 20 GHz.

The **linear amplifier** applications of HBT can be found in both receivers and transmitters. For receiver application, the third-order products must be minimized at the lowest dc bias points. A figure-of-merit number, IP3/dc power, often used to quantify the usefulness of devices for these applications, can be very high for HBTs. In transmitters, the linearity is better measured as the ratio of carrier to intermodulation products (C/I) from two-tone tests near 1-dB compression point. Impressive results have been obtained with HBTs in the latter application at 7.5 GHz with 20 W internally matched amplifiers[4].

The **wideband amplifier** applications of HBT have been gaining popularity since the demonstration of a 45% efficient, 1W amplifier covering the 8 - 14 GHz range[5]. Other

amplifiers for the 7-11 GHz [6]and 6-18 GHz bands[7] have been successfully fabricated. In this application, the lower Q-value of the HBT input and output impedance is useful for efficient impedance matching capability. The high power density is also important to maintain a small device size and more favorable impedance conditions for wideband matching.

As commonly encountered with all new device technologies, the HBT had to overcome several materials growth, fabrication, and reliability concerns to achieve the level of maturity it now enjoys. Several alternative techniques exist to address the materials growth and fabrication processes. The main materials growth technique is MOCVD, which is now commercially available from several vendors. But, MBE and MOMBE are also applicable for some lower power devices. The fabrication techniques are many and varied, but the essential process components are identical to those used for other GaAs devices, such as FETs.

The reliability is a major concern for all power devices, and HBT is no exception to this rule. Since 1989, when the first reliability data became available, good progress has been made to identify and eliminate degradation mechanisms that cause long term reliability in power amplifiers. Because HBT is a minority carrier device, its degradation mechanisms are related to material defects and the non-radiative recombination that occurs at these defects. Projected device lifetimes as high as 1E7 hr have been predicted from measured data[8]. Continuing improvements in materials and processing techniques are expected to further increase the reliability.

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MOVPE Growth and Characterization of Carbon-Doped $In_{0.47}Ga_{0.53}As$/InP HBT

A. Wiersch, A. Lindner, Q. Liu, F. Scheffer, D. Peters, W. Prost, E.Kuphal*, F. J. Tegude

Gerhard-Mercator-University Duisburg, Sonderforschungsbereich SFB 254,
Solid-State Electronics Department, D-47057 Duisburg, Germany
*Deutsche Telekom Research Institute, D-64295 Darmstadt, Germany

ABSTRACT:

Very high carbon doping of p-$In_{0.53}Ga_{0.47}As$ is the key issue for a reliable high speed Heterostructure Bipolar Transistor (HBT) on InP-substrate. We will report on our experimental work using the metalorganic vapor phase epitaxy (MOVPE) approach for carbon doping of $In_{0.53}Ga_{0.47}As$ with CCl_4. Based on this work and the current literature [e.g. 1, 2] we will present a model which describes the technological features with special emphasis on the impact of hydrogen (H^+) on carbon incorporation and passivation in p-$In_{0.53}Ga_{0.47}As$. Our model of carbon doping in $In_{0.53}Ga_{0.47}As$ is based on one fundamental assumption: p-type doping is achieved by cracking group III precursors (TEGa + TMIn) and avoiding the desorption of the carbon containing molecules by using chloride simultaniously. Chloride coming from cracked CCl_4 acts as a strong H^+-ion getter reducing the desorption of CH_x molecules from the growth front, increasing the available carbon concentration above the growth front. Highly p-doped $In_{0.53}Ga_{0.47}As$ (hole concentrations above $1\cdot10^{19}cm^{-3}$)achieved if the H^+-atoms are avoided or gettered.

Using the H^+ getter approach by Cl from CCl_4 or Br from CBr_4 extremly low growth temperatures are required regardless of the used method [1,2] which imply substantial problems for the HBT technology like growth temperature profiles including long growth interrupion times, mass controlled layer growth causing problems concerning layer homogeniety or carbon passivation by growing with Hydrides. Hence we will address the expectations of H^+-avoidance (e.g. the replacement of hydrides) in the frame of our model.

Carbon-Doped $In_{0.47}Ga_{0.53}As$/InP HBT were grown using a low temperature MOVPE process for the p-doped $In_{0.47}Ga_{0.53}As$ base layers. We will describe our experiences concerning process parameters for HBT growth with special emphasis on temperature profiles and annealing experiments for overcoming the H^+ passivation of the carbon doped base layers in HBT.

Temperature dependent DC characterization of HBT will be presented including detailed parameter extraction using sophisticated simulation and modeling methods based also on RF results.

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GaAlAs/GaAs and GaInP/GaAs HBT's for power applications

J.P.Bailbé, J.Tasselli, L.Andrieux, H.Granier, T.Camps, A.Cazarré, A.Marty, M.Faleh

Laboratoire d'Analyse et d'Architecture des Systèmes du CNRS
7, Avenue du Colonel Roche
31077 TOULOUSE Cedex - France

In the HF power transistors domain, GaAlAs/GaAs heterojunction bipolar transistors present very promising results compared to silicon structures; their potentialities for amplifying power have been widely discussed. We present the frequency and power performances obtained from large devices (emitter finger area of 10x200 μm^2), our aim being the design and fabrication of a power amplifier MMIC. Thermal problems are also investigated.

We have compared two types of structures: GaAlAs/GaAs Be-doped HBT's (MBE-grown) and GaInP/GaAs C-doped transistors (MOCVD-grown). The two structures are fabricated using a standard mesa technology: the only difference in the technological process steps concerns the emitter mesa definition. A dry etch ($SiCl_4$-RIE) is performed for GaAlAs, a selective wet chemical etch (H_3PO_4/HCl etchant) is used for the GaInP layer. Power devices being interdigitated, a 2 µm-thick gold metallization is sputtered over the emitter contacts, by using the air bridge technology (figure 5). This allows the reduction of the longitudinal emitter resistance[1] and the improvement of the heat dissipation, avoiding hot spot formation. The influence of thermal coupling mechanisms among neihboring fingers, which is a limiting factor for performance of multiple emitter HBT, can be minimized.

Typical (Ic,Vce) output characteristics are reported in figure 1 for one emitter-HBT. The current gain is 70 for GaAlAs/GaAs HBT and 50 for GaInP/GaAs. The first one is more sensitive to self heating occurring at high collector current levels.

Small signal S-parameters measurements carried out on a single emitter HBT exhibited at Ic=100mA a f_T of 20 GHz and fmax of 13 GHz for GaAlAs/GaAs system, and f_T=8 GHz and f_{max}=11 GHz for GaInP/GaAs (figure 2).

Power measurements were performed on discrete GaAlAs/GaAs HBT's. Output powers of 0.63 W with a power added efficiency (PAE) of 58% and a power gain of 10 dB are obtained at 2 GHz (figure 3). Performances at 4 GHz are an output power of 0.7 W with a PAE of 55% and a power gain of 4 dB.

Thermal characterization of GaAs based power transistors is becoming increasingly important for circuit design [2,3], a problem with technology being the low thermal conductivity of GaAs. If we consider high power densities (>10^4 W/cm²) and interdigitated structures, the estimation of thermal resistance is no more sufficient, and it is necessary to use a numerical program which solves the three dimensional heat transfer equations. Temperature dependence of thermal conductivity is solved using the Kirchoff transformation [3].

Examples of simulated results obtained for a 4-emitter fingers transistor are reported in figure 5, about the influence of substrate material on the temperature dependence. Two structures are studied: a typical GaAs semi-insulating substrate and a diamond substrate acting as a chip carrier (we suppose that the HBT device thinned down to 3 µm is attached to diamond by the way of ELO method [4]). The thermal conductivity of the diamond is higher than for GaAs (19 W/°C.cm versus 0.46 W/°C.cm at ambient temperature).

The transversal repartition of temperature shows that, for power fixed at 1 W, the HBT temperature drops from 220°C for a GaAs substrate (figure 4a) down to 30°C for a diamond substrate (figure 4b). This shows the importance of developing new technologies and new designs to solve the thermal problem in GaAs power HBT's.

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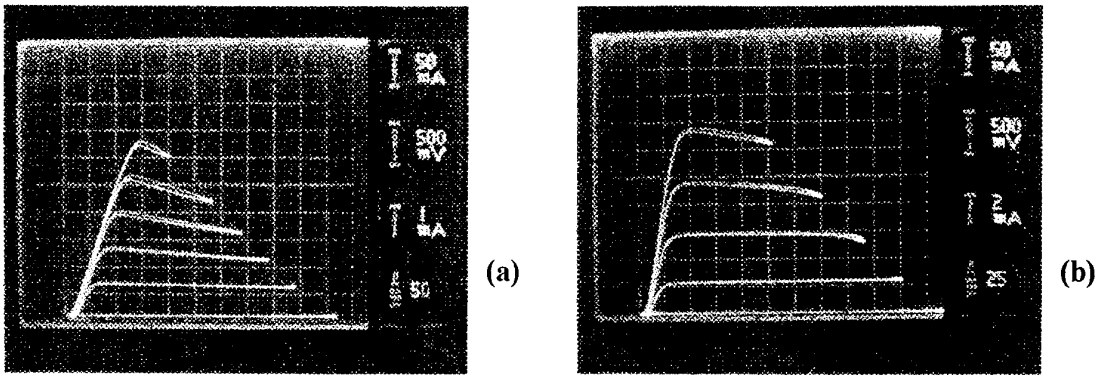

Figure 1: (Ic, Vce) characteristics of GaAlAs/GaAs (a) and GaInP/GaAs (b) HBT

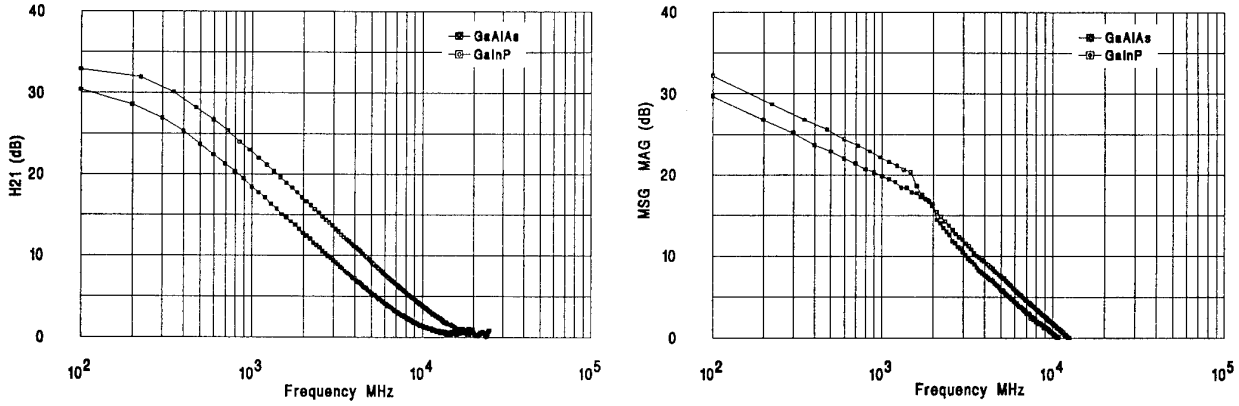

Figure 2: Current gain and power gain versus frequency for one emitter HBT at Ic=100mA

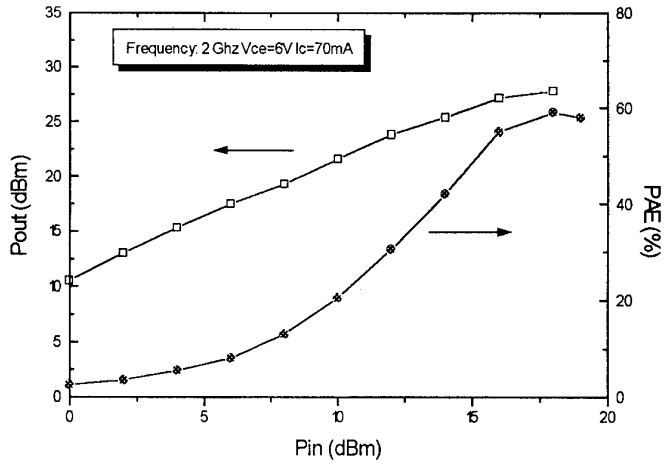

Figure 3: Output power and power added efficiency for GaAlAs/GaAs HBT

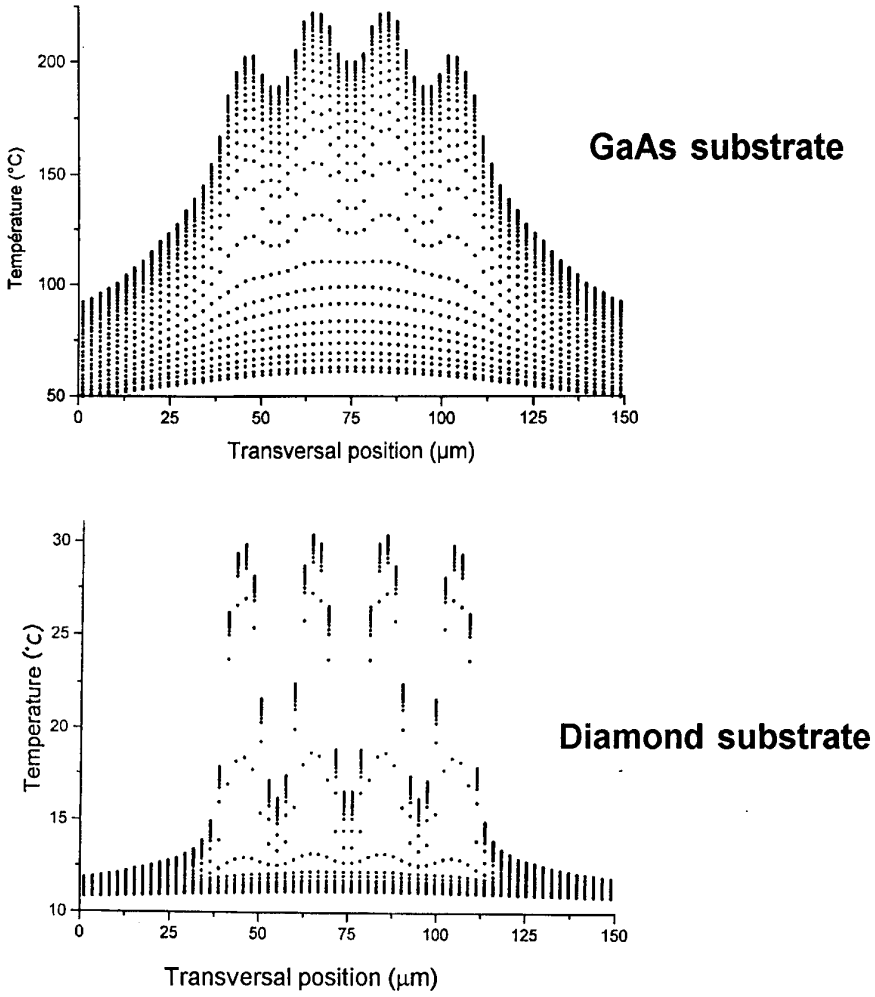

Figure 4: Transversal repartition of temperature for a 4-emitters HBT

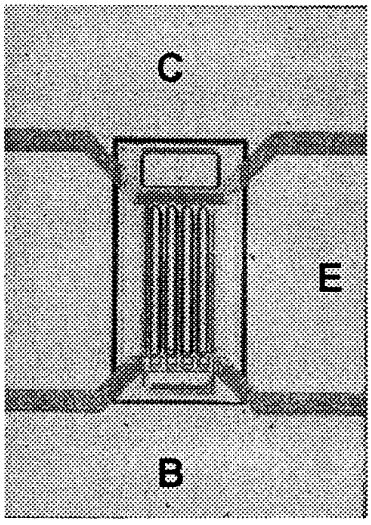

Figure 5: Photograph of a 4-emitter fingers HBT

Hole Barrier Bipolar Transistors using InGaP/GaAs

by

Carlos Saavedra-Muñoz*, D.W. Woodard*, K. Whittingham*, L.F. Eastman*, and L.W. Yang+

* *School of Electrical Engineering . Cornell University . Ithaca, New York.*
+ *Electronics Laboratory. Lockheed-Martin Corporation. Syracuse, New York.*

In this paper we will concentrate in the electron and hole transport at the emitter-base junction of a Hole Barrier Bipolar Transistor (HBBT) using the InGaP/GaAs material system. The concept behind the HBBT is that instead of making the entire emitter of the bipolar transistor of a wide band-gap material as in the HBT, only a thin spacer layer of the wide band-gap material is placed between the base and emitter of the device. The size of the valence-band discontinuity is very critical because it must be large enough to prevent hole tunneling into the emitter. We will specifically look at hole tunneling and how it affects the emitter efficiency of the device. At stake is whether the probability of light-hole tunneling is large enough to be comparable to the electron tunneling, in which case using a spacer layer over a wide band-gap emitter may be detrimental to device performance. Finally, the results will also shed light on the dopings that will be possible in the base and emitter regions of the device for a given spacer thickness.

The numerical calculations are based on a one-dimensional thermionic emission model. The conduction band discontinuity is taken to be 1/7 of the valence band discontinuity, which for the InGaP/GaAs material system is 0.42 eV. The emitter and base dopings are in the 5.0×10^{17} cm^{-3} and 1.0×10^{19} cm^{-3} range, respectively. The barrier is 200 Å thick, made of intrinsic InGaP. At Cornell we have fabricated devices with these characteristics, and they have a high gain: 76 at Vce = 3.0 V and base currents of 100μA. Theoretical and experimental results will be presented.

HOT ELECTRON NOISE IN AN AlGaAs-BASED TRIPLE-HETEROJUNCTION CHANNEL

A.Matulionis, V.Aninkevičius, V. Bareikis J.Liberis, I.Matulionienė
Semiconductor Physics Institute, A.Goštauto 11, Vilnius LT-2600, Lithuania

P.S.Kop'ev, V.M.Ustinov
A.F.Ioffe Physico-Technical Institute, St. Petersburg 194021,Russia

High-speed performance of a field-effect transistor is often achieved at a cost of excess noise. Since the Nyquist relation fails at high electric fields, data on channel noise are not available from other than noise measurements [1].

The equivalent noise temperature of hot electrons is determined by measuring the noise power emitted by an ungated channel into a waveguide at 10 GHz at 80K.

A triple-heterojunction structure consists (Fig.1, from right to left) of a high-purity GaAs, a thin (2.5 nm) undoped AlAs spacer, a 1 nm planar-doped GaAs layer, and an undoped AlGaAs layer [2]. It has a high-mobility high-density channel in the undoped GaAs. The AlAs spacer is inserted to reduce real-space transfer of hot electrons. The δ- doped GaAs layer is so thin, that the lowest subband of the left-hand well is located well over that in the right-hand well (Fig.1).

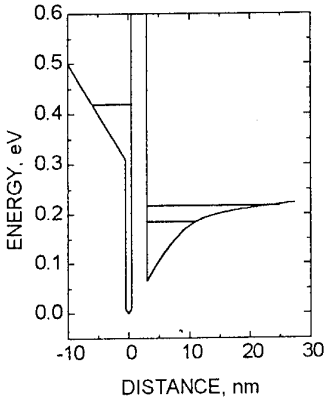

Fig.1. Band structure of the AlGaAs / δ- GaAs / AlAs / GaAs triple-heterojunction channel [2].

The hot electron noise due to real-space-transfer fluctuations are found to dominate in AlGaAs/GaAs channels at fields below the threshold for the intervalley noise in GaAs (2 kV/cm) [2]. Exploitation of AlAs spacer in channel C leads to the highest threshold field for the real-space transfer (Fig.2). The noise temperature is rather high in long channels (Fig.2), and dependence of the real-space transfer noise on the channel length is to be considered.

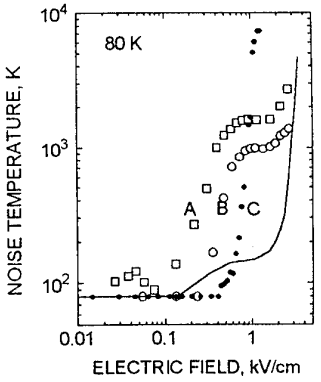

Fig.2. Noise temperature for AlGaAs-based channels (Table 1) and high mobility GaAs (solid line, 77000 cm^2/Vs) at 80 K [2].

Table 1. Heterostructure channel parameters [2].

Channel	AlGaAs/GaAs		AlGaAs/GaAs/AlAs/GaAs
	A	B	C
Al ratio in spacer	0.25	0.33	1.0
Spacer thickness, nm	3	40	2.5
Electron density, $10^{11}cm^{-2}$	5.7	1.9	13
Electron mobility, cm^2/Vs	75000	103000	35000
Sample length, μm	20	7.5	18

Fig.3. presents the noise temperature for 18 μm and 3 μm triple-heterojunction channels. The dependence on the channel length is quite impressive: the noise temperature is suppressed by over 15 dB at 1.2 kV/cm when the channel length is reduced from 18 μm to 3 μm.

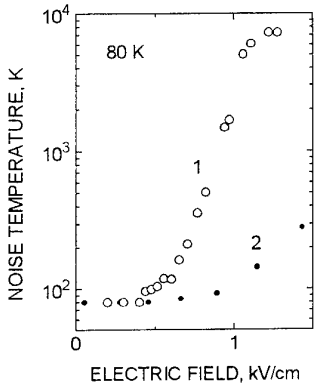

Fig.3. Noise temperature at 80 K for the channels C (Table 1) of different length:
1- 18 μm, **2** - 3 μm [2].

Fig.4 illustrates dependencies of the hot electron noise temperature on the channel length when the measurements are taken at a fixed electric field. The data for the triple-heterojunction chan-nel (Fig.4, points 3) taken from Fig.3 (at 80 K at 1.2 kV/cm!) are compared to those for uniformly doped GaAs investigated at 300 K at 4 kV/cm (Fig.4, points 1 and 2).

It is noteworthy, that the curves of Fig.4 cross. For example, at the fixed 4 kV/cm field long lightly doped channel of GaAs shows a higher noise temperature as compared to the long doped GaAs channel (Fig.4, Points 1 and 2). However, the opposite is true for the 1 μm channels (Fig.4). These results confirm the expectations that shorter lengths are required for suppression if the scattering is heavy. The triple-heterojunction channel has the highest mobility and the longest critical length among the channels of Fig. 4.

Thus, the threshold field for the real-space transfer noise is the highest in the triple-heterojunction channel. This source of noise is suppressed in short channels.

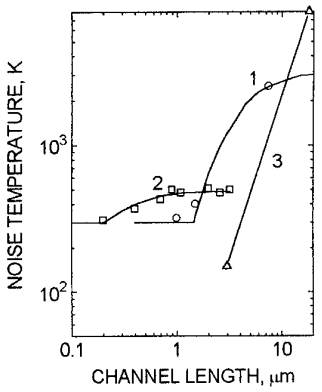

Fig.4. Dependence of the noise temperature on the channel length at the fixed electric field [1,2].
1 - lightly doped GaAs, 4 kV/cm at 300 K, μ_0 =7500 cm^2/Vs.
2 - doped GaAs, 4 kV/cm, 300 K, μ_0 = 3900 cm^2/Vs.
3 - channel C, 1.2 kV/cm at 80 K, μ_0 = 35000 cm^2/Vs.

Acknowledgments

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Noise in Channel Doped GaInP/InGaAs-HFET-Devices

D. Geiger*, E. Mittermeier*, J. Dickmann°, C. Geng+, R. Winterhoff+, F. Scholz+, E. Kohn*

*Department of Electron Devices and Circuits, University of Ulm

°Daimler-Benz Research Center Ulm

+4 th Phys. Institute, University of Stuttgart

Germany

Channel doped GaInP/InGaAs structures have been grown by low pressure MOVPE on GaAs substrate. We fabricated recessed HFET devices with a gatelength of 0.25µm and a self-aligned ohmic contact enhancement to reduce the parasitic resistances. As the conduction band offset of the GaInP/GaAs heterointerface is low, a channel doped approach was used to obtain a high current density, instead of following the conventional HEMT approach. The selective etching of the GaAs against the GaInP provides a technological advantage concerning homogenity and yield. As a result we have obtained a high current density of 500mA/mm in combination with an extrinsic peak transconductance of 550mS/mm, a transit frequency of 68GHz and a maximum frequency of oscillation of 160GHz.

On these devices microwave noise measurements and low-frequency noise measurements were carried out at different drain currents.

From microwave noise measurements, we obtained a minimum noise figure of 0.6dB with an associated gain of 13dB at 12GHz. The increase of the noise figure with frequency was very weak, and the noise figure at 26GHz was still below 1dB. This low noise figure is attributed to a reduction of the parasitic resistance but also to the high valence band offset of the GaInP heterostructure, which reduces the hole induced gate leakage current. The low noise figures also indicate, that the device performance is not degraded by a possible reduction of the mobility by the channel doping. The lowest noise figure was obtained at a drain current of 100mA/mm, corresponding to 20% of the maximum drain current, but the noise figure increases very slowly with drain current. Additionally, the increase of the noise figure with drain current was accompanied by an increase of the associated gain up to 85%I_{DSmax}. At a drain current of 350mA/mm, corresponding to 70% of the maximum drain current, the noise figure was still below 1dB at 12GHz. These low noise figures at high currents are due to a reduced conductivity in the GaInP even at high currents because of the channel doped approach.

Low frequency noise measurements were carried out between 10Hz and 1MHz. The noise spectrum indicates a pure 1/f noise spectrum in the entire frequency range. In contrast to conventional PM HEMTs with AlGaAs as barrier layer, no Lorentzian shaped generation recombination noise was observed. This indicates the absence of DX-centers in the GaInP. As in the case of microwave noise, the low-frequency noise showed only little dependence on the gate bias, which again illustrates the low conductivity in the GaInP even at high currents.

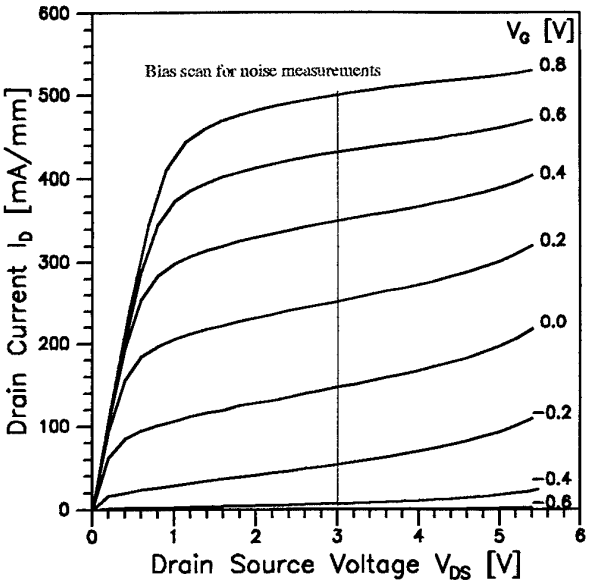


Fig. 1: DC-characteristic of the channel doped GaInP/InGaAs HFET. The line illustrate the bias range, over which the noise figures were measured.

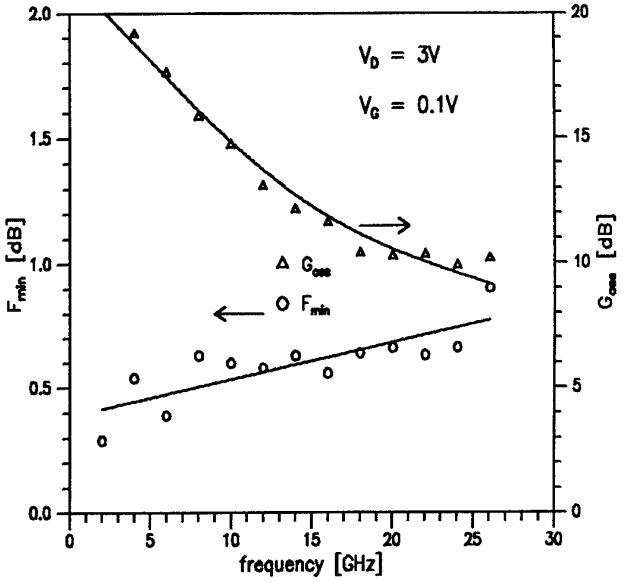


Fig. 2: Noise figure and associated gain between 2GHz and 26GHz. The drain current is 100mA/mm, corresponding to 20%I_{DSmax}.

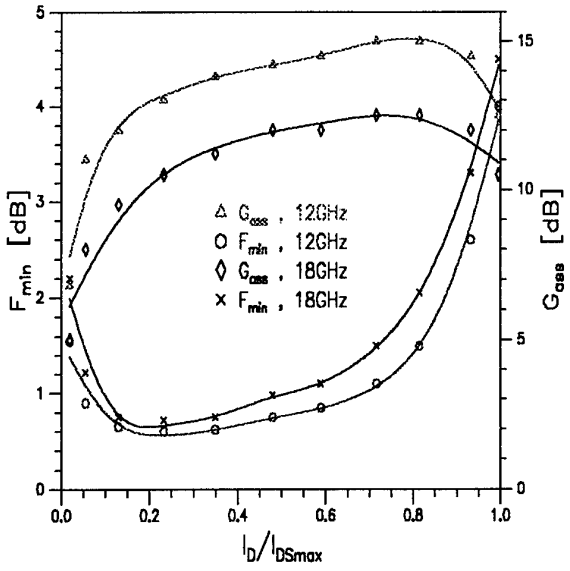


Fig. 3: Dependence of the microwave noise and associated gain on drain current.

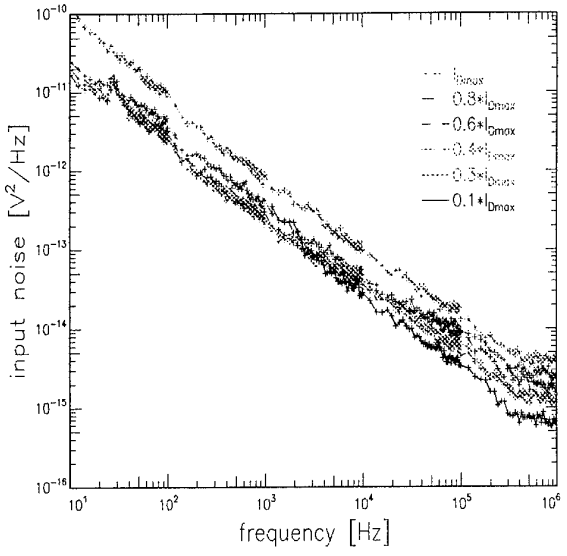


Fig. 4: Low-Frequency noise spectrum at different drain currents.

ISOTHERMAL ELECTRIC BREAKDOWN IN MESFET AND MODFET

Ya.B. Martynov and A.S. Tager.

SR&PC 'Istok',
Fryazino, Moscow region, 141120, Russia.

Power and reliability of transistors are restricted by an irreversible breakdown which leads to a semiconductor structure burnout. As far as we know the physical picture of this breakdown have not been completely cleared up today. Many experimental facts and especially short times ($t < 1$ ns.) of the destructive breakdown in the modern FETs with effective heat sinks show that this burnout is initiated not by semiconductor heating but by some cumulative isothermal process.

In report some results of computer simulation of the isothermal breakdown in the GaAs MESFET and in the GaAs\InGaAs MODFET are presented. The simulation was based on the non stationary hydrodynamic model. A new completely stable, efficient difference scheme was used. This scheme allowed us to speed up the calculations essentially by using rough grids with large steps in space and time as well as mixed boundary conditions - constant given potentials at source and gate and given drain full current .

Computer simulation showed that irreversible breakdown in MESFETs can be caused by the isothermal formation of S-type source-to-drain C-V characteristic leading to current filamentation. These processes are initiated by the electron accumulation and a high electric field domain formation near the drain. Holes created in this domain by the impact ionization are injected into the i-type substrate and move to the source. Being accumulated at i-n junction near the source these holes induce an additional electron injection into the substrate providing there a low field quasineutral region. Therefore the increase of the drain current caused by the increase of electric field in the high field domain near the drain is accompanied by the decrease of the potential drop between source and drain and hence - by decrease of source-to-drain voltage. When negative gate voltage increases, the critical 'turn point', where the source-to-drain conductance becomes negative, shifts to large drain voltages due to the high field domain widening to the gate. If negative gate voltage is large enough the impact ionization will begin near the gate leading to the increasing of the gate current. If the gate sustains this current then further increasing of drain voltage will stimulate the avalanche carrier multiplication near the drain and cumulative carrier accumulation which leads to S-type C-V characteristic formation as it is described above.

In MODFET heterobarriers make carrier escape from the channel more difficult and hence prevent the development of described cumulative processes and S-type instability. Therefore MODFET can be more stable relative to irreversible breakdown than MESFET.

A new equivalent MESFET circuit is proposed which takes into account the processes at large source-to-drain voltages and can be successfully used in the well known SPICE program.

SESSION 7

PROCESSING

Dry etched Fabry-Perot (FP)-{110} facets of 1.55 μm (RW)- laser

K.Vogel, J.Würfl
Ferdinand-Braun-Institut für Höchstfrequenztechnik Berlin
Rudower Chaussee 5
12489 Berlin, Germany

RW-laser diodes based on InGaAsP/InGaAs-MQWs grown by chemical beam epitaxy (CBE)* have been successfully fabricated by using reactive ion etching (RIE) for defining the laser facets (Fig.1). The influence of the process parameters of the methane/hydrogen RIE process for facet definition on the threshold current, vertical far field and the etching induced optical damage was studied. A comparative study was carried out for three types of RW-laser diodes with resonator lengths of 400μm and 600 μm (both sides cleaved, one side etched one side cleaved, both sides etched, Fig.2). It is shown that the use of hydrogen-containing gases in RIE-processes leads to a reduction of activated acceptors in p-doped layers on the facet surface and to a formation of a polymer layer coating the masked regions of the structure. Also thin polymer layers could be observed on the {110}-facets. The lift-off structured Ti/Pt/Au/Ti-p-type contact pads act as a resistant etching mask with very smooth edges, better than λ/10. An ohmic contact behavior after annealing including a defect deactivation in p-doped layers was observed. Polymer-coated facets have been cleaned in oxygen-RIE mode and in combination with a chemical etch step in HF : H_2O (1 : 4) for several times. The laser characteristics in dependence on the device processing will be discussed. Tab. 1 lists some laser data for 4μm wide RW structures (5 kHz:500ns) without facet passivation.

Facet preparation (C:cleaved, E:etched)	threshold current i_s (mA)	optical power P (mW) 100mA	optical power P (mW) 200mA	vertical far field
C - C	20-40	60	155	34
C - E	30-50	20	25	36
E - E	40-80	10	12	39

This work has been supported by the Deutsche Bundespost Telekom.
* The quantum well laser structures were grown at the Tampere University of Technology, Department of Electrical Engineering, Physics, Finland

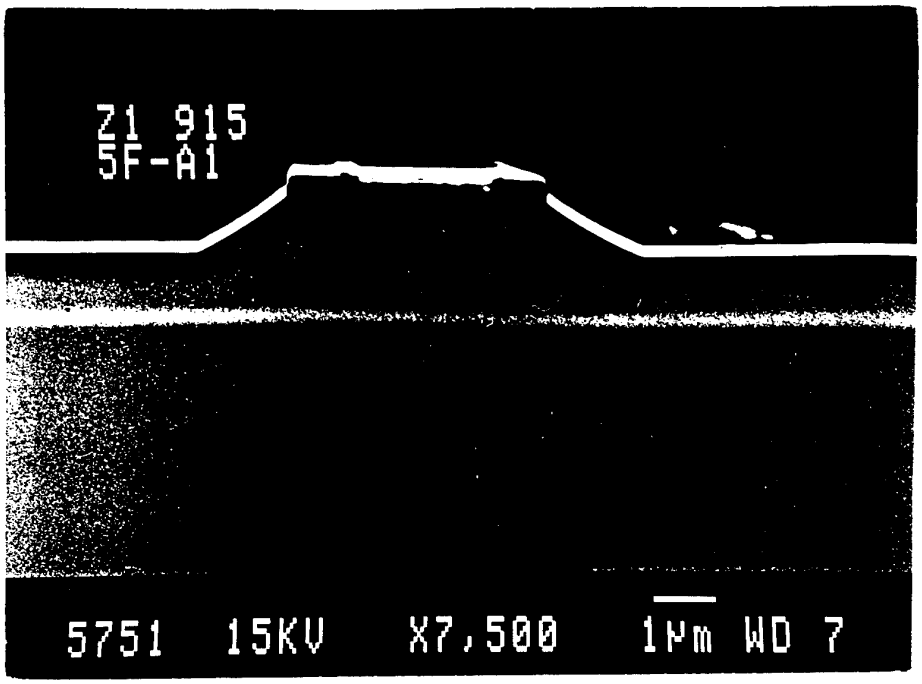


Fig. 1
Scanning electron microscope (SE-mode) picture of cross-section of 4 μm width RW laser structure

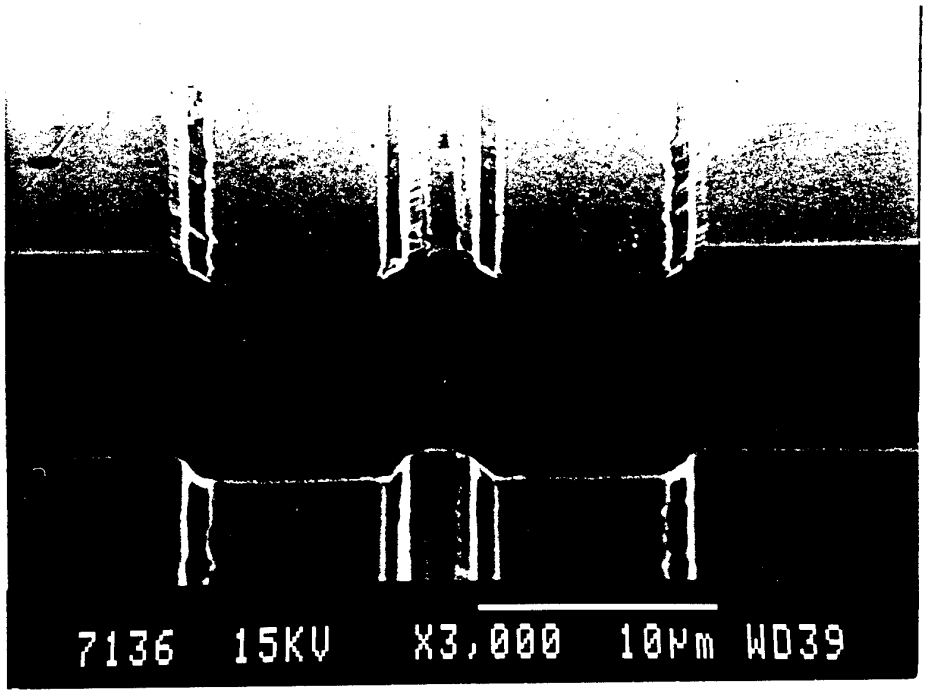


Fig. 2
Scanning electron micrograph of 1.55 μm RW-laser facets fabricated by methane/hydrogene RIE

ENHANCED CHEMICALLY-ASSISTED ION-BEAM ETCHING PROCESS FOR HIGH-SPEED GaAs-BASED MQW LASERS

R. E. SAH, J. D. Ralston, K. Eisele, S. Weisser, and W. Benz

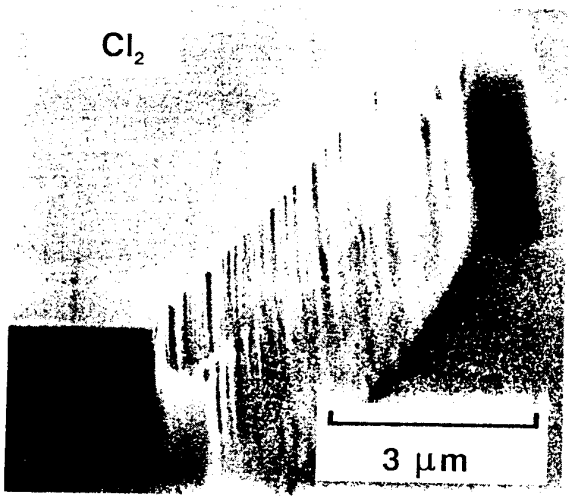
Fraunhofer-Institut für Angewandte Festkörperphysik,
Tullastrasse 72, D-79108 Freiburg, Germany

Chemicaly-assisted ion-beam etching (CAIBE), using an Ar ion beam and Cl_2 as the reactive etching gas has received considerable attention in dry-etching of compound semiconductor devices. The technique offers reasonably independent control of physical and chemical components of the etch process and allows high etch rate, while yielding low residual damage. However, internal cold traps, elevated substrate temperatures, and multilevel dielectric or metal masks have been found necessary in order to achieve sufficiently high and reproducible etch rates along with smooth vertical etch profiles. These restrictions presented a particularly severe challenge for the vertically-compact high-speed MQW laser structures $In_{0.35}Ga_{0.65}As/GaAs/Al_xGa_{1-x}As$ containig high-Al-mole-fraction ($x_{eff} \leq 0.8$) epilayer, developed in our laboratory [1]. Due to the very high affinity of Al in the $Al_xGa_{1-x}As$ layers for any oxygen arising from residual O_2 or H_2O in the etching chamber aluminum oxide is readily formed, which can not be etched easily, and therefore leads to rough stepped surfaces (Fig. 1). We have developed an enhanced CAIBE process [2], using an Ar ion beam and $Cl_2 + BCl_3$ reactive etching gases. This technique relaxes these constraints and allows to fabricate highly anisotropic and step-free etch profile (Fig. 2) at substrate temperature of only 60° C, and using the standard photoresist as an etch mask. Using this process we have fabricated dry-etched mirrors in MBE-grown undoped and p-doped $In_{0.35}Ga_{0.65}As/GaAs$ strained-layer MQW laser structures containing high-Al-mole-fraction cladding layers. Fig. 3 presents the modulation response of 3x100 μm^2 ridge waveguide devices with undoped and p-doped active regions, demonstrating modulation bandwidths of 24 GHz at a DC bias current of only 25 mA and 33 GHz at a DC bias of ony 65 mA for undoped and p-doped devices, respectively.

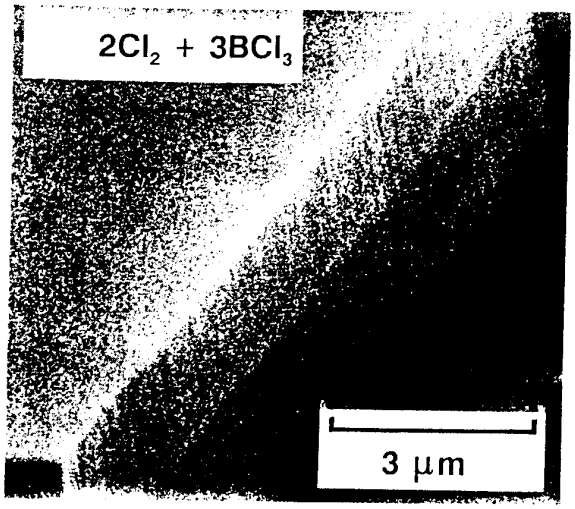
The single facet optical output power, P for 3x100 μm^2 lasers with undoped and p-doped active regions is plotted in Fig. 4 as a function of the drive current, I. In both cases, the P-I curves are linear up to single facet optical output powers of at least 6 mW. Corresponding far-field measurements demonstrate single lateral mode output for drive currents up to 50 mA for both, the undoped and p-doped devices.

[1] J.D. Ralston, S. Weisser, K.Eisele, R. E. Sah, E.C. Larkins, J. Rosenzweig, J. Fleissner, and K. Bender, IEEE Photon. Technol. Lett. **6**, 1076 (1994).

[2] J. D. Ralston, K. Eisele, R. E. Sah, S. Bürkner, J. Fleissner, K. Bender, E. C. Larkins, and S.Weisser, Technical Digest: 1994 LEOS Summer Topical Meeting on Optoelectronic Materials Growth and Processing, pp. 24-25.



▲ **Fig. 1** SEM micrograph of etch facet in $In_{0.35}Ga_{0.65}As/GaAs$ MQW structures containing high-Al-mole-fraction cladding layers etched by classical CAIBE technique using Cl_2 as reactive gas (Ar=5 sccm, U=450 V, T= 60° C, Photoresist).



▲ **Fig. 2** SEM micrograph of etch facet in $In_{0.35}Ga_{0.65}As/GaAs$ MQW structures containing high-Al-mole-fraction cladding layers etched by CAIBE technique using $Cl_2 + BCl_3$ as reactive gas (Ar=5 sccm, U=450 V, Cl_2 =2 sccm, BCl_3 = 3 sccm, T= 60° C, Photoresist).

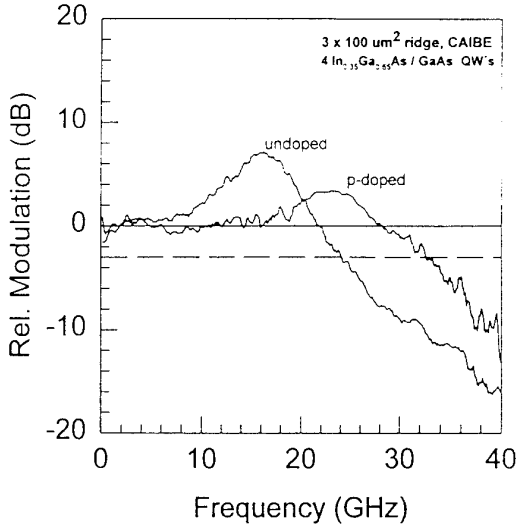


Fig. 3 Modulation response of 3x100 μm^2 ridge waveguide lasers with 4 undoped and p-doped $In_{0.35}Ga_{0.65}As/GaAs$ quantum wells (uncoated facets, heat sink temperature = 25° C). DC bias currents were 25 mA and 65 mA for devices with undoped and p-doped active regions, respectively.

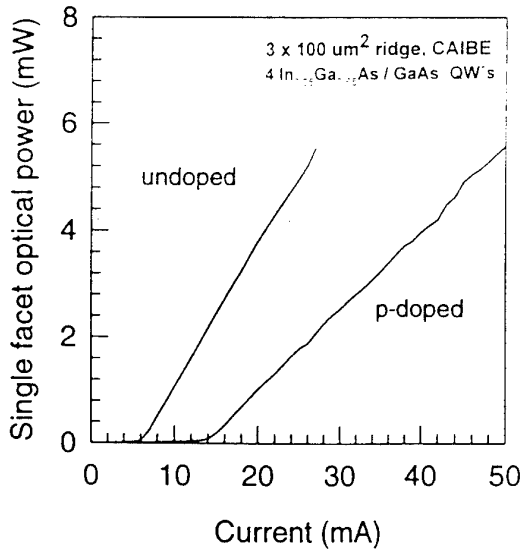


Fig. 4 CW single-facet optical output power vs. current for a 3 x 100 μm^2 $In_{0.35}Ga_{0.65}As/GaAs$ ridge waveguide lasers with undoped and p-doped active regions.

The influence of $CH_4/H_2/Ar$ ECR plasma etching on GaAs-based heterostructures for field effect transistors

J.G. van Hassel, C.M. van Es*, P.A.M. Nouwens* and L.M.F. Kaufmann.
COBRA Inter-University Research Institute on Communication Technology,
Eindhoven University of Technology, Department of Electrical Engineering,
Den Dolech 2, P.O.Box 513, 5600 MB Eindhoven, The Netherlands
* Department of Technical Physics, Semiconductor Physics group

Abstract

Electron Cyclotron Resonance (ECR) plasma etch processes using $CH_4/H_2/Ar$ have been optimised for gate recessing in heterostructure field effect transistors. The influence of this plasma is investigated by I-V and C-V measurements on Schottky diodes and on AlGaAs/GaAs and AlGaAs/InGaAs/GaAs heterostructures by Hall measurements.
The passivation depth is determined as function of the GaAs doping level by C-V measurements. Recovery of the electrical activity of the passivated donor atoms was obtained after annealing at 400 °C for 1 minute. A slight degradation in the I-V characteristics of Schottky diodes could be observed as function of increasing process bias. If the GaAs toplayer of an AlGaAs/GaAs heterostructure was removed by plasma processing, the Hall mobility was restored for 74 percent after annealing at a measurement temperature of 5.6 K, compared to a wet chemically etched reference sample. The 2-DEG sheet density fully recovered. However if a Si δ-doped layer is incorporated in the heterostructure the Hall mobility and the sheet density completely restored after the plasma treatment and subsequent annealing. In these experiments a minimal damage was observed after processing at an process bias of -40 Volt. Identical experiments on AlGaAs/InGaAs/GaAs pseudomorphic heterostuctures even showed a more pronounced influence of an additional δ-doped layer. It seems that such a layer prevents further introduction of damage into the semiconductor material. The results were compared to those obtained with conventional CH_4/H_2 Reactive Ion Etching (RIE) on the same layer structures. Finally the DC and high frequency characteristics of wet chemically processed pseudomorphic HFETs were compared to those having a dry gate recess.

Investigation of CH_4/H_2 RIE for gate recess etching in InGaAs/InAlAs-based HEMTs

H.C. Duran and W. Patrick

Laboratory for Electromagnetic Fields and Microwave Electronics
Swiss Federal Institute of Technology Zürich
ETH-Zentrum, CH-8092 Zürich, Switzerland
Tel.: +41 - 1 - 632 76 25
Fax: +41 - 1 - 632 11 98
email: duran@ifh.ee.ethz.ch

We present a methane-hydrogen RIE process for gate recess etching of lattice-matched InGaAs/InAlAs/InP-HEMTs without inducing measurable electrical damage into the channel layer. The use of an Atomic Force Microscope (AFM) allows precise control of the morphology of the etched 0.2 μm gate recess.

The accurate definition of the gate recess in MESFET and HEMT devices is important to ensure uniform and reproducible device parameters. For low feature sizes, wet etching techniques suffer from surface wetting problems which reduce the uniformity of the devices. Dry etching techniques can provide much more controllable etching characteristics.

Halogen-based chemistries, hydrocarbon chemistries and mixtures of both have been used for dry etching InP-based materials. Chlorinated gases cannot be used at substrate temperatures around 300 K due to the low vapor pressure of the $InCl_x$ etch products. Bromide-based gases like HBr are more suitable for etching but they are extremly environment unfriendly. We concentrated on methane-hydrogen Reactive Ion Etching (RIE) because these gases are nontoxic and satisfactory etching characteristics can be achieved at room temperature.

A major problem of hydrocarbon-based etch chemistries is the deposition of a polymer layer on non-etching surfaces. The AFM profile in figure 1 shows that a polymer is built up on the InAlAs Schottky layer after removing the 10 nm thick InGaAs cap layer of the HEMT structure in a plasma with 23.2% CH_4 concentration. An ashing step in an oxygen plasma reveals the true etch depth which is deeper than the cap layer (fig. 2). The polymer formation strongly degrades the uniformity of the device parameters. We cannot perform an ashing step to remove the polymer after gate recess etching because we use a self-aligned lift-off process with a three-level PMMA/P(MMA-MAA)/PMMA resist structure for T-shaped gate definition. Reducing the CH_4 content in our plasma to 8.3% and the power to 20 W, we could achieve a selectivity of 100 between the etch rates of InGaAs and InAlAs (fig. 3). AFM images showing the morphology of the gate recess will be presented.

HEMTs etched at low power with dc bias voltages below 200 V showed no increase in sheet resistance even after 500% of overetching. There was no need for an additional oxygen plasma treatment after gate recess etching or for an annealing step after gate metallisation to restore the carrier concentration. The devices had electrical parameters comparable to those obtained by wet etching in phosphoric acid but with a much higher uniformity. The standard deviation over 22 dry-etched HEMTs on one sample was 5% for the peak transconductance g_{mmax}, 40 mV for the threshold voltage V_{th} and 4% for the drain current I_{dss} at $U_{gs} = 0$ V. Similar results were achieved on other device runs. The corresponding standard deviations for the wet-etched HEMTs varied between 8% and 18% for g_{mmax} and I_{dss}, and 100-350 mV for V_{th}. Microwave measurements showed a unity current gain frequency f_t of 120 GHz and a unity power gain frequency f_{max} of 220 GHz for a HEMT with 150 μm gate width.

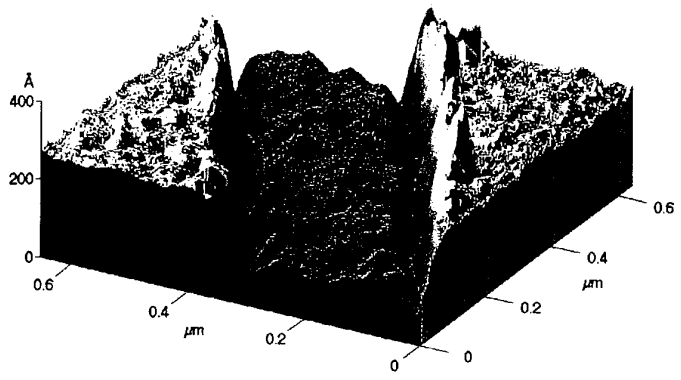


Fig. 1: Gate recess etched with 23.2% CH_4 at 35 mtorr and 30 W RF power after resist removal.

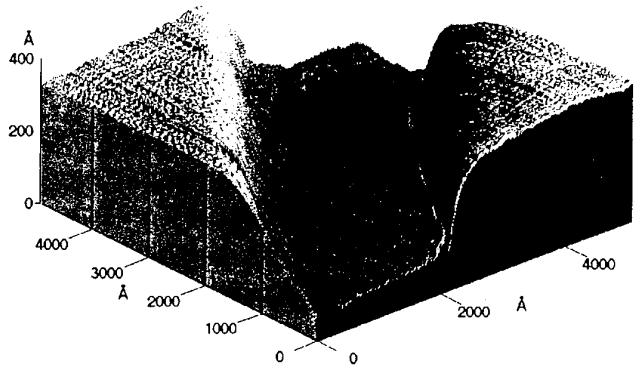


Fig. 2: The same recess as in figure 1, but after an oxygen plasma treatment.

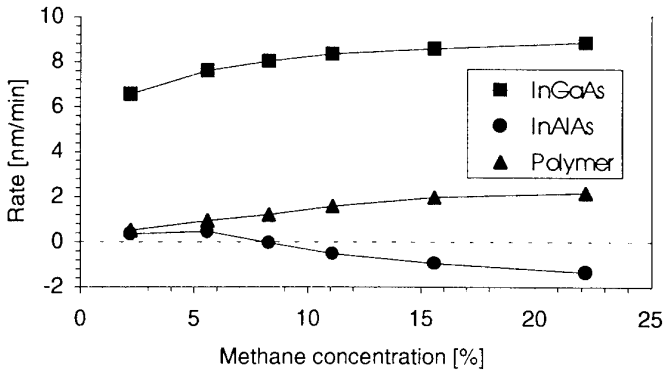


Fig. 3: Etching rates of InGaAs and InAlAs and polymer deposition rates in a methane-hydrogen plasma at a pressure of 35 mtorr, 20 W RF power and a total mass flow of 90 sccm.

High Barrier Schottky Contacts on n-InP using Damage Free Electrochemical Metallization

D. C. Dumka, R. Riemenschneider, J. Miao, H. L. Hartnagel
Institut für Hochfrequenztechnik
Technische Hochschule Darmstadt
Merckstraße 25, D-64283 DARMSTADT, Germany
and
B. R. Singh
Central Electronics Engineering Research Institute
PILANI-333 031, India

Abstract

Due to the well known superiorities of InP over GaAs such as higher electron velocity, better thermal conductivity, higher breakdown field and lower surface recombination velocity, it has been considered to be very attractive for electro-optic and microwave applications. In addition, a favourable realization of the high-quality lattice-matched compound semiconductor material systems such as InP/InGaAs/InP, it is of much interest for the photonic devices. However, due to the poor properties of the native oxide layer on the n-InP which causes strong pinning of the Fermi level near the conduction band, it has been quite a challenging task to fabricate good quality rectifying Schottky contacts on it. Fabrication of Schottky contacts on n-InP by means of conventional metal evaporation techniques results in a very low barrier height, high ideality factor and high leakage current even at a very small reverse bias. The damage of metal/InP interface during the metal evaporation process and the presence of native oxide at the interface are the main reasons for such poor results.

Electrochemical deposition of metal on GaAs has been widely reported in literature. This novel technique offers *in-situ* etching of the semiconductor surface just prior to the metallization. During the etching process the electrolyte/semiconductor interface is biased by voltage pulses in the avalanche region which consequently etches the native oxide present on the surface of the semiconductor. Metallization is carried out by just changing the polarity and the parameters of the voltage pulses while the sample is kept in the electrolyte. Hence, re-oxidation of the semiconductor surface is prevented. Moreover, the metallization process itself is very soft which produces a damage-free metal/semiconductor interface.

We have studied and optimized this novel metallization technique which first has been reported by N.-J. Wu *et. al.* (1994), to realize the Schottky barrier contacts on n-InP with Platinum as the contact metal. Bulk n-InP with (100) orientation and carrier concentration of $3x10^{15}$ cm^{-3} was used for our experiments. The Pt-bath consisting of H_2PtCl_6, H_2SO_4, and H_3PO_4 was taken as the electrolyte. Dot-structure Schottky diodes with varying radius from 25μm to 500μm were fabricated. The *in-situ* etching of InP and Pt deposition were carried out by a voltage pulse generator using the pulse

amplitude between 10V to 20V, width between 0.2 μs to 10μs and repetition rate of 1mS. The pulse etching was preceded by surface chemical etching of InP in HF and HCl solutions.

The fabricated Schottky diodes were analyzed by IV, CV, DLTS, and XPS characterization. The barrier height obtained from IV and CV measurements was 0.64eV and the ideality factor was found to be 1.01. DLTS measurements of Pt/InP interface showed no prominant peaks which confirmed the damage-free metal/InP interface.

In order to establish the feasibility of the process for real device applications, metal-semiconductor-metal photodetector (MSM-PD) structures were realized on the same n^-InP material. The MSM-PDs consist of back-to-back biased and planar interdigital Schottky barrier contacts on the semiconductor. Such photodetector structures on InP/InGaAs/InP material are of significant importance for the long wavelength optical communication systems. We have fabricated MSM-PDs with an active area of 100x100 μm^2. Low dark current between 20 nA to 40 nA and capacitance between 0.7pF to 0.8 pF at 6V bias were obtained.

In the present paper we report on the process optimization, the results which have been obtained for Schottky barrier contacts on n^-InP using the methods described above and a comparison of electrochemical and electron-beam evaporated Pt/n^-InP Schottky contacts. Additionally, we present the significance of the novel process towards the fabrication of InP based MSM-PDs .

Ohmic Contact Degradation in AlGaAs/GaAs HEMTs

W. T. Anderson[1], K. A. Christianson[1], and C. Moglestue[2]

1) Naval Research Laboratory, Code 6855, Washington, DC 20375
202-767-1755, fax: 202-767-0455

2) Fraunhofer Institute, Freiburg, Germany
49-761-5159-535, fax: 49-761-5159-400

ABSTRACT

Reliability studies were made of 0.3 μm gate length AlGaAs/GaAs high electron mobility transistors (HEMTs) to determine if the same failure mechanisms would be present under differing life test stress conditions. For this purpose the devices were life tested under high temperature storage, dc bias, and dc bias with 1 dB compression RF conditions. It was determined that the failure mechanisms do differ significantly, and that the ohmic contacts degrade more rapidly under RF life testing.

For each life test stressing condition described above three stress temperatures were used. A minimum of five devices were examined for each stress temperature of a given stress condition. The failure criteria was chosen to be a 20% decrease in the saturated drain current at zero gate bias (I_{DSS}) as measured at the life test temperature. For all life testing conditions a decrease in transconductance along with a shift of the maximum transconductance to more positive gate voltages accompanied the I_{DSS} decreases. As Fig. 1 illustrates for averaged data, the high temperature storage devices had the largest shift of maximum transconductance, while all devices showed comparable decreases in transconductance. Monte Carlo modeling was used to simulate a number of different possible failure mechanisms in order to explain these changes. Transconductance depression was found to be related to ohmic contact damage, while the shift of the maximum transconductance was found to reflect gate sinking.

Ohmic contact and channel resistance measurements for the same set of devices are shown in Table I. The change of channel resistance was found to be greatest for the high-temperature storage devices. This is explicable in that gate sinking is a thermal diffusion process, in contrast to the field aided diffusion possible for the dc or dc+RF stressed devices. The change of drain resistance for the dc+RF stressed devices was found to be greater than the change of drain resistance for the dc stressed devices. This difference reflects the importance of hot carriers at the drain due to the increased electric field from the RF, as predicted by the Monte Carlo simulations.

To our knowledge, these are the first reported Monte Carlo simulations of Ohmic contact in HEMTs. In this model, Ohmic contact resistance is assumed to result from electrons tunneling through the AuGe/Ni alloy/N^+-GaAs interface. The tunneling probability is calculated by solving the Schrodinger equation for each electron, whose path through the device is simulated by the Monte Carlo method. Calculated increases in the Ohmic contact resistance resulting from RF life testing agree with the measured values within 20 %.

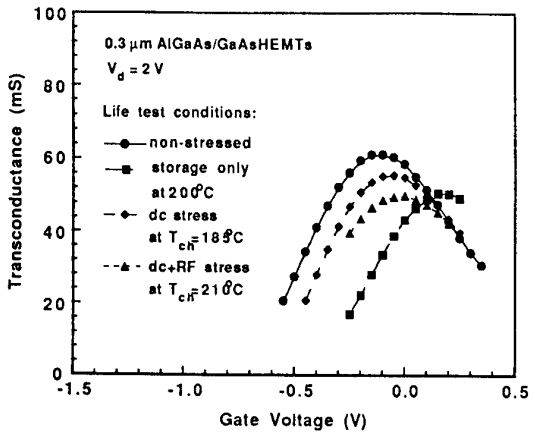


Fig. 1. Transconductance versus gate voltage as a function of stressing conditions for the life tested AlGaAs/GaAs HEMTs.

Life test type	R_S (Ω)	R_D (Ω)	R_{CH} (Ω)
Before life test	3.6	2.9	1.4
Storage test (200°C)	4.5	4.8	2.8
dc life test (185°C)	4.3	5.0	1.3
dc+RF life test (210°C)	4.9	7.8	1.2

Table I. Ohmic and channel resistance as a function of stressing conditions for the life tested AlGaAs/GaAs HEMTs.

Comparison of AuGe/Ni ohmic- and Ti Schottky-contact on n^+-GaAs for rf-power generation above 140 GHz

J. Freyer, M. Tschernitz, Technical University of Munich

The main problems for the power generation at elevated mm-wave frequencies result from rf-impedance matching and from ohmic losses of the active device and the used resonator. Recently a module encapsulation technique for active two-terminal devices has been developed which offers a powerful tool for a reproducible matching whereby at the same time the parasitic elements can be minimized [1]. This technique is applied to investigate the ohmic losses of GaAs transit-time devices with different contacts in the frequency range above 140 GHz. The active device chosen is a double-Read Impatt diode structure from which rf-output power up to 160 GHz can be obtained [2]. In Fig. 1 the diode structure with the different layers is shown. In this paper, the influence of the contact at the n^+-layer side on rf-output power and maximum frequency is investigated.

For contacts on highly doped GaAs n^+-layers normally the well-known AuGe/Ni contact system is used which delivers a specific contact resistance below $10^{-6}\ \Omega cm^2$, a relatively low value which, however, is measured only at dc or low rf-frequencies. As an alternative to the AuGe/Ni ohmic-contact, in this paper a Ti Schottky-contact is investigated. For the normal reverse bias of the Impatt diode, the Schottky-contact is forward biased and can be described as a parallel circuit of a conductance and a capacitance. The conductance is proportional to the current density and the capacitance depends on the corresponding forward voltage and the doping concentration of the contact layer. For a typical n^+-doping density of about $2 \cdot 10^{18}\ cm^{-3}$ and a current density between 10 $kAcm^{-2}$ to 100 $kAcm^{-2}$, the real part of the parallel-circuit impedance can be estimated to values between $1 \cdot 10^{-6}\ \Omega cm^2$ and $1 \cdot 10^{-7}\ \Omega cm^2$ for frequencies between 140 GHz and 160 GHz.

GaAs double-Read Impatt diodes after Fig. 1 were fabricated from one batch with AuGe/Ni- and Ti Schottky-contacts on the n^+-contact layer, respectively. The fabrication of the active devices with module encapsulation structure is described elsewhere [1]. The rf-output power measurement results are shown in Fig. 2. It can be seen that the devices with Ti Schottky-contact can generate up to 100 mW output power at a frequency of 145 GHz and the maximum oscillation frequency is 164 GHz. For the devices with AuGe/Ni ohmic-contact 100 mW output power could be achieved only at 132 GHz and the highest frequency is reduced to 158 GHz. The results point out that the losses for the devices with AuGe/Ni contact are higher as compared to the Ti Schottky devices. Therefore, the minimum threshold current density for oscillation (a direct measure for the losses in resonator and diode) of the different devices is investigated . The results are plotted in Fig. 3. It can be seen that the minimum current density of the Ti Schottky devices is always lower as compared to the AuGe/Ni devices. The total specific rf-losses calculated from the values of Fig. 3 by the help of a small-signal computer simulation lead to an equivalent series resistance of about $4 \cdot 10^{-6}\ \Omega cm^2$ for the Ti Schottky-contact devices which is a reduction of about 30 % as compared the devices with AuGe/Ni ohmic-contact.

In conclusion, by the help of GaAs double-Read Impatt diodes it has been shown that for elevated mm-wave frequencies the contact resistance on highly doped n^+-GaAs can be reduced if instaed of the well-known AuGe/Ni contact a Ti Schottky-contact is applied. The active devices with this contact lead to higher rf-output power and higher oscillation frequency. An estimation of the total losses at mm-wave frequencies shows that the losses can be reduced by about 30 %.

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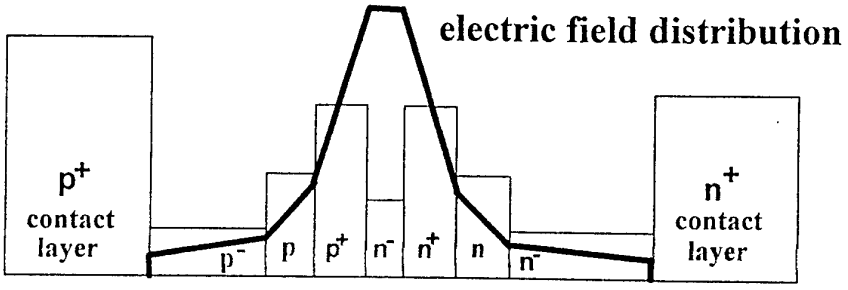

Fig. 1: GaAs double-Read Impatt diode structure with principal electric field distribution

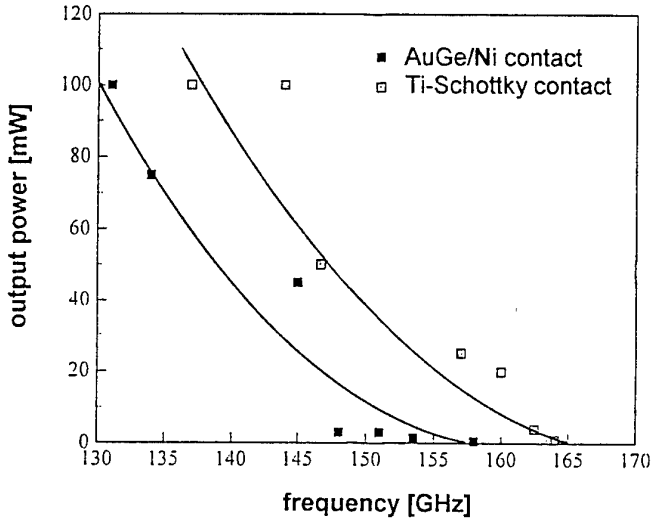

Fig. 2: Output power versus frequency for double-Read Impatt diodes with AuGe/Ni- and Ti Schottky-contact

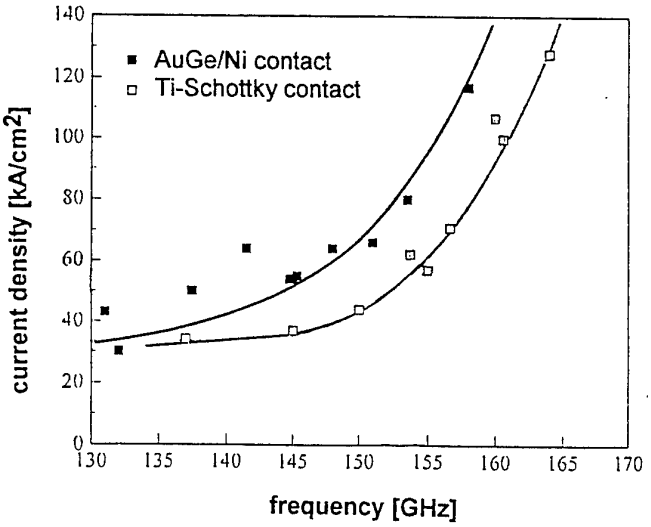

Fig. 3: Minimum threshold current density versus frequency for double-Read Impatt diodes with AuGe/Ni- and Ti Schottky-contact

Metallizations for GaAs MMICs operating at elevated temperatures up to 300°C

J. Würfl, E. Nebauer, U. Merkel, K. Vogel

Ferdinand-Braun-Institut
für Höchstfrequenztechnik Berlin
Rudower Chaussee 5
12489 Berlin - Germany

Tel: +49-30-6392-2690
Fax: +49-30-6392-2642

MMICs designed for continuous operation at high temperatures require metal/semiconductor transitions and metallic interconnections on chip that facilitate good electrical performance over the whole temperature range and high reliability at elevated temperatures. For high temperature stable devices the following requirements have to be met: i) metallurgical inert metal/semiconductor contacts, ii) low specific contact resistivity of the ohmic contacts, iii) Schottky contacts employing a high potential barrier (important for high temperature MESFETs and HEMTs), and iv) high overall conductivity of the contact system to avoid resistive losses in the circuits.

One approach to solve these problems simultaneously will be presented in this paper. The idea is to consequently separate electrical and metallurgical functions of a metal/semiconductor contact. This is accomplished by three different types of metallic layer systems that are stacked one over the other. The electrical performance of the contact system is mainly determined by the choice of the first layer arrangement in intimate contact with the semiconductor and its processing technology . This metallic system has to be either thermodynamically stable to GaAs or may, depending on processing conditions, even react with the semiconductor in a controlled and predictable manner. It will be shown that for high-barrier Schottky contacts to GaAs (Φ_B ~ 0.85 eV) Pt-type materials such as Pt, Ir and interstitial rare earth compounds such as LaB_6 can be used whereas internal thin layers of NiAuGe or PdInGe may form one component of high temperature stable ohmic contacts. The second layer system acts as a diffusion barrier that metallurgically separates the often poorly conducting inner system from a third, highly conductive metallic system on top of the contact. The thicknesses of the individual layers are chosen in such a way that the complete contact represents a nearly ideal electrical semiconductor/metal transistion (ohmic or Schottky type) while maintaining a high overall conductivity. The diffusion barrier consists of an amorphous WSiN layer that has been reactively sputtered from a W-Si mosaic target in Ar^+-N^+ atmosphere. The highly conductive metallization is formed by a thick Au overlay on top of the WSiN.

A systematic optimization of different Schottky and ohmic contact systems together with long term life time tests at temperatures up to 400°C has led to metallic contacts that meet the aforementioned requirements. The development of the metallizations has been accompanied by electrical tests, and material analytic techniques such as SNMS, AES, cross sectional TEM and X-Ray diffraction. GaAs-MESFETs fabricated by using optimized metallic systems have been successfully operated between liquid nitrogen temperature and 500°C (see Figure 1).

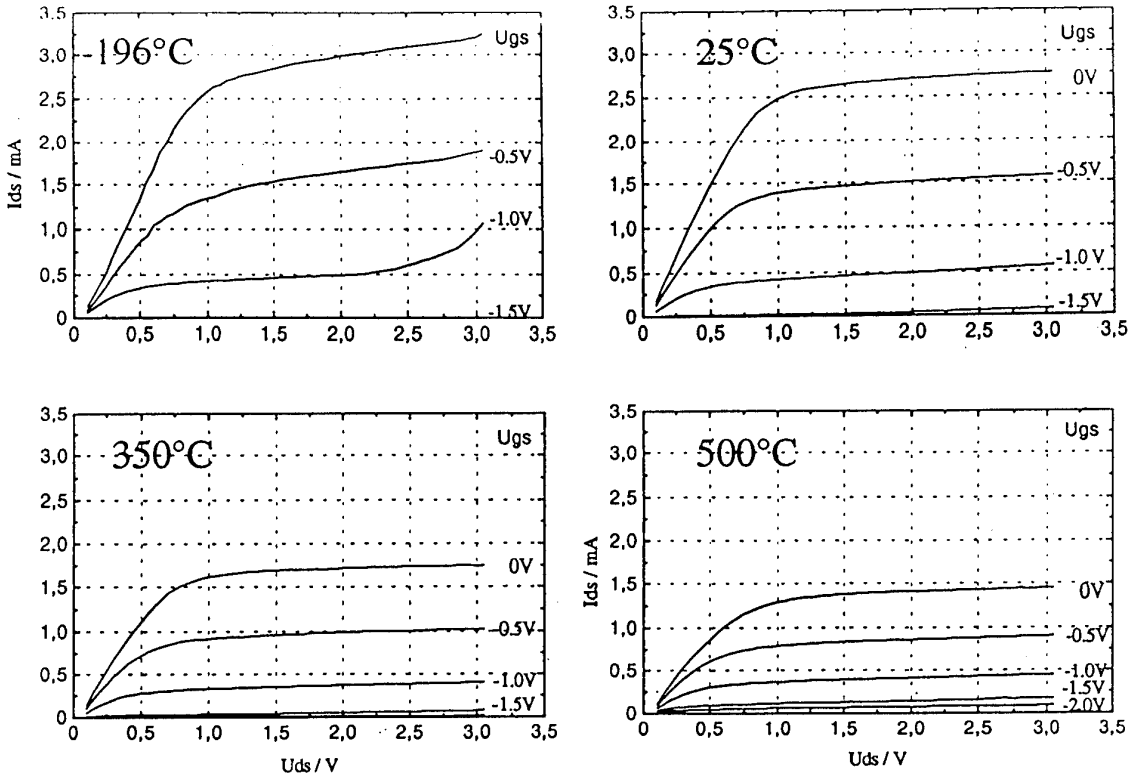

Figure 1: Output characteristics of a GaAs-MESFET operating at -196°C, 25°C, 350°C and 500°C. (Gate length: 0.5µm; Gate width: 10µm)

WEDNESDAY

SESSION 8

TRANSISTORS II

GaAs-MMIC Applications in Wireless and Fiber Optic Telecommunication Systems.

Mikael Snellman
Ericsson Components

The first large volume commercial applications for GaAs monolithic microwave IC's, MMIC's were in Television Receive Only (TVRO) and Ku-band Direct Broadcast by Satellite Television (DBS-TV) systems which emerged in the second half of the 80's. These circuits showed the feasibility of GaAs-MMIC technology for high volume, low cost commercial applications. Once the potential of MMIC had been realised, the interest in exploring its possibilities in other areas increased. Having since long been accepted by the military for low volume, high performance and price applications, GaAs-MMIC's now find their way into consumer electronics, where pricing pressures are intense.

The main commercial applications for GaAs are: mobile communication, satellite receivers, fiber-optic communication and wireless data communication. The largest volumes by far are expected in mobile handsets. There are a lot of technologies competing to find a place in this area: Si(BIP, MOS, BiCMOS, SiGe) and GaAs(MESFET, HBT, HEMT) in Hybrid as well as in MMIC configurations. Due to the varying systems demands it is believed though, that no one technology will dominate and that all are likely to play a role.

The power amplifier, PA, is a key standard handset product. For low power, a few watts, MMIC's are rapidly gaining ground. The main advantage for GaAs in this area is the high power added efficiency which improves battery life time. For the Transmit/Receive switching function many systems use GaAs, which offers the high isolation and low current needed. In the receiver front-end GaAs faces stiffer competition, Si BiCMOS being a strong threat.

In fiber optic communication GaAs MMIC's play the traditional role of performing the critical front-end functions: driving the laser diode and acting as a low noise transimpedance amplifier for the photo detector current. Si is probably competitive up to about 1 Gbps. At higher frequencies GaAs has an advantage in lower noise and a higher tolerance to variations in packaging and diode properties.

MMIC's offer a combination of smaller size, lower cost and better performance. But MMIC's are not always the best choice. Since development costs of MMIC's are usually high, the cost benefits are only realised in high production volumes. Furthermore the performance of an MMIC is a compromise. Hybrids can be tuned for optimum performance, MMIC's can not. The design must be made so as to accommodate process variations at the price of performance.

Some people believe that one-chip solutions will be the most cost efficient. Others claim that one-chip solutions will be too poor, and prefer to use multi-chip solutions where the most appropriate technology can be chosen for each function.

GaInP/GaAs HBT MMIC POWER AMPLIFIERS AT X-BAND

H. Blanck, S. L. Delage, D. Floriot, S. Cassette, E. Chartier,
M-A. di Forte-Poisson, D. Pons, P. Roux*, E. Watrin*, P. Chaumas*, P. Bourne*

THOMSON-CSF / Laboratoire Central de Recherches - F-91404 Orsay Cédex.
* THOMSON-CSF / TCS - BP 46 - 91401 Orsay Cédex.
FRANCE

Heterojunction bipolar transistors (HBT) have a strong potential for high-power, high-efficiency microwave amplifier applications, and quite a few impressive results have been published using the AlGaAs/GaAs system [1,2]. The GaInP/GaAs heterostructure is emerging as a very promising alternative [3,4]. Among other things we can mention etching selectivity, favorable band-gap line-up and improved low frequency noise characteristics as strong advantages of this material system.

We used Thomson's self-aligned GaInP/GaAs HBT process [4] to fabricate the amplifiers reported in this paper. The structures were MOCVD-grown, and we used C dopant for the base layer in order to achieve very high doping levels with minimum diffusions. Typical values for the base sheet and contact resistances are 130Ω/square and $5.10^{-2}\Omega.mm$ respectively. Emitter fingers are $2x30\mu m^2$, and a single-finger device exhibits F_T and F_{max} around 55GHz and 100GHz, extrapolated from S-parameter measurements. For power amplifiers we use 4, 6 or 8-finger cells depending on the required output power. The unit-cell so-called fishbone layout has been optimized for X-band operation, with a 32μm inter-finger spacing. The figure 1 shows the CW power performance of a 8-finger device at 10GHz. The power added efficiency reaches 48% for an output power of 0.6W in class A operation. In order to ensure thermal stability the devices have internal and external ballast resistors.

We present here the results obtained on two single-stage amplifiers. Circuit 1 consists of eight 6-finger unit-cells, and the chip size is $3.6x5.1mm^2$. Figures 2 and 3 show, as a function of frequency and input power, the output power (Pout) and power added efficiency (PAE) of this circuit. These results are obtained under pulsed conditions (10μs pulse, 10% duty cycle) including tuner losses. At 9GHz Pout reaches 4W, and PAE 43%. For circuit 2, using eight 8-finger unit-cells and a more compact layout, we achieved 5W of output power and 32% of PAE (figure 4). The chip size is only $3.1x5.1mm^2$, and is shown in figure 5. A better understanding of the non-linear behavior of our devices and a reduction of their thermal resistance should allow us to improve these results. However, they already confirm that GaInP/GaAs HBTs are a strong candidate for power amplifiers.

This work is supported by the French department of Defense (DRET) and inside the European consortium IEPG-TA1 CTP 1.8.2. The author would especially like to thank their Daimler-Benz colleagues for all the technical exchanges during the last years.

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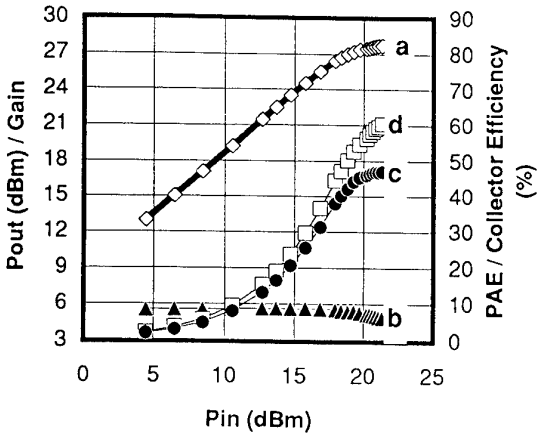

Fig. 1: CW power performance of a 8-finger HBT at 10GHz
a- Pout b- Gain c- PAE d- CE

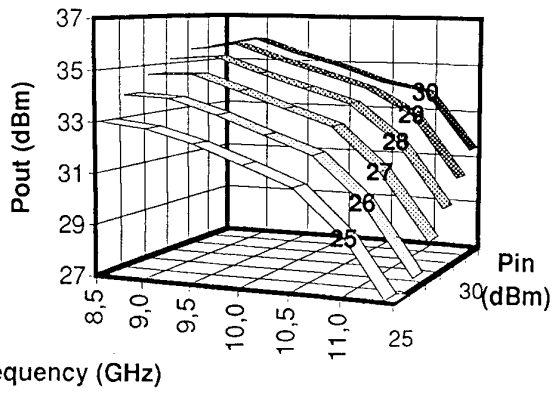

Fig. 2: Output power versus frequency and input power under pulsed conditions (10µs, 10%). Circuit 1

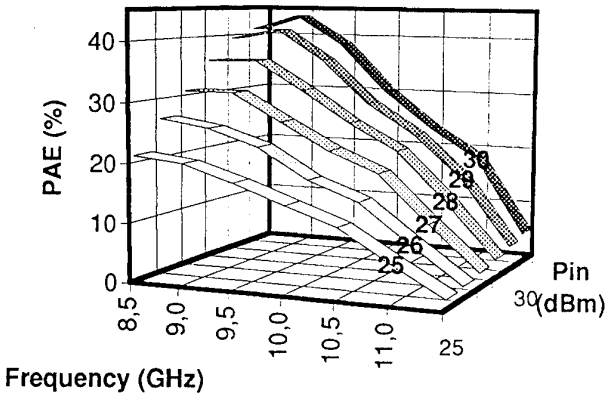

Fig. 2: Power added efficiency versus frequency and input power under pulsed conditions (10µs, 10%). Circuit 1

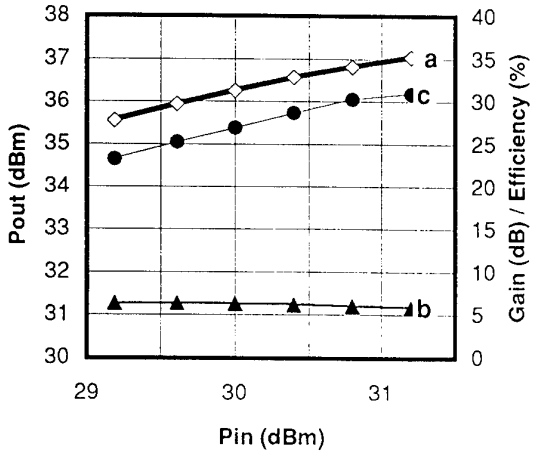

Fig. 4: Power performance of Circuit 2 under pulsed conditions at 9.5GHz (10µs, 10%).
a- Pout b- Gain c- PAE

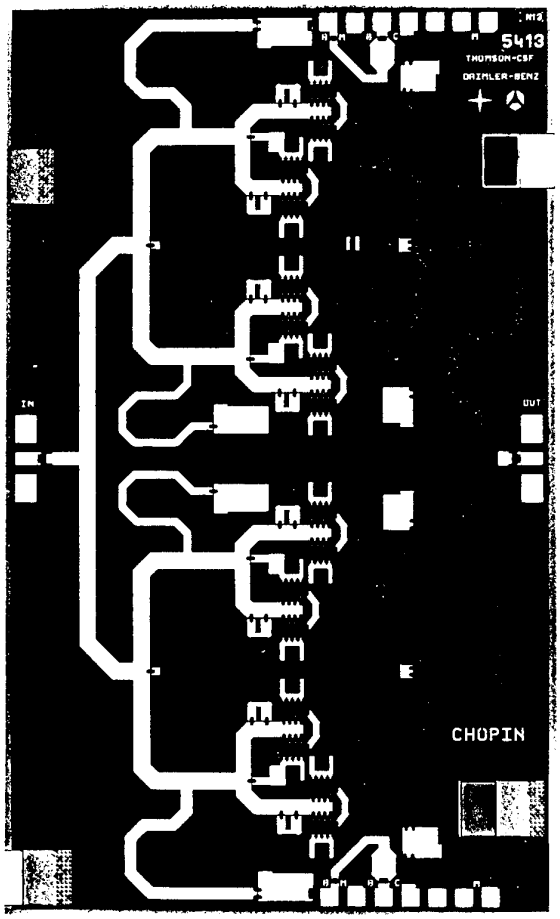

Fig. 5: Photograph of a single-stage HBT X-band power amplifier (Circuit 2). Chip size is 3.1x5.1mm2

Advanced PMHFET GaAs MMIC components for Ka-band communication systems

P.Narozny, H. Dämbkes, J.M. Dieudonnne'*, B.Adelseck*

Daimler Benz Research Center, Wilhelm Runge Straße 11, 89081 Ulm, Germany
Daimler Benz Aerospace AG, Woerthstraße 85, 89070 Ulm, Germany

A number of civil applications such as motion sensors and communications systems are planned to use Ka-Band frequency range. Millimeter-wave MMICs are attractive for new communications systems from the following point of view:

- compactness
- enhancement of links performances
- decrease of the production costs
- increase of the reliability

The key MMIC circuit functions for Ka-Band communication systems have been fabricated. Low noise amplifiers, voltage controlled amplifiers, a medium power amplifier and different mixers have been developed using a common 0.25µm PMHFET technology allowing a future integration of several key components on a single chip.

The 0.25µm PMHFET transistor technology has been established to provide state of the art low noise and power devices. For this purpose a single planar doped single heterojunction structure has been chosen. The transistors show a typical f_{max} of 160 GHz and a minimum noise figure of 0.8dB at 18 GHz.

Low noise amplifier
A low noise amplifier has been fabricated using 0.25µm PMHFETs. The stability was achieved by inductive series feedback. Furthermore it was possible to achieve simultaneous noise and input power matching. In order to obtain a broadband circuit with high gain a tree stage amplifier has been chosen. The measurement results demonstrate a gain of 18dB associated with a noise figure of 3dB in the frequency range 32GHz-40GHz.

Variable gain amplifier
A gain controlled amplifier has been developed by replacing the single gate transistor in the last stage of the previous low noise amplifier by a dual gate cascode transistor. The gain is controlled by the voltage applied to the second gate of the dual gate transistor. A gain of 18dB with a dynamic range of more than 25dB has been obtained. The input and output return losses is better than 10dB over the complete dynamic range and the frequency band of 32GHz to 40GHz.

Medium power amplifier
The power amplifier was designed as a two stage balanced amplifier. The balanced configuration has been realized by using Lange coupler at the input and output. The circuit exhibits an output power of 23dBm and a gain of 10dB combined with return losses better than 15dB over the frequency band 26GHz-40GHz.

Mixer
Three different mixers have been fabricated. PMHFET Schottky diodes, single gate transistor and dual gate transistors have been used as mixing elements. The circuits have been designed using large signal simulation on a commercial simulator. The obtained results will be presented in the talk.

Compact High Gain Low Noise 60 to 80 GHz Amplifiers on GaAs

Jürgen Braunstein, P.-J. Tasker†, M. Schlechtweg†, H. Maßler†,
A. Hülsmann†, K. Köhler†, W. Bronner†, and Jo. Schneider†
Cornell University, School of El. Engineering, Phillips Hall, Ithaca, NY 14853-5401
J. Braunstein is on leave from the †Fraunhofer Institute for Applied Solid State Physics, Tullastrasse 72, D-79108 Freiburg, Germany
Phone +1 (607) 255-1432, Fax +1 (607) 255-4742
E-mail: jurgen@iiiv.tn.cornell.edu

Abstract

Very compact 2-stage narrow band LNAs with more than 20 dB gain between 60 and 80 GHz have been fabricated using cascodes as active elements. On wafer S-parameter measurements showed a maximum gain of over 30 dB at 67 GHz. To the best of our knowledge this is the highest gain ever reported for a two-stage LNA in that frequency range. CPW technology is used to allow for dense packing of the various circuit elements. The chip size including all matching and bias networks is only 0.59 mm · 1.4 mm (0.83 mm^2).

Introduction

Increasing interest for high frequency applications, i.e., collision avoidance radars at 60 and 76 GHz, is obvious. There are considerable advantages in cost and development time if the mature GaAs MMIC technology can be utilized for these frequencies. However, simulations for LNAs in the millimeter-wave and ultra high frequency domain have shown that circuit design is severely hindered by the high feedback value of standard HEMTs on GaAs. A gain element like the cascode solves the problem allowing for sufficient amplification with low noise properties. A cascode is the series connection of two transistors where the input transistor is operated in common source configuration and the output transistor in common gate configuration. The gate of the second transistor is capacitively grounded and can be used for gain control. In this configuration the effective feedback capacitance is minimized by reduction of the Miller feedback effect [1]. Since the cascode is nearly unilateral, it is an ideal gain element for amplifier design [2].

LNA design

The design was optimized for high gain from a small chip area to keep costs low. Pervious high gain designs with standard HEMTs achieved 31.7 dB gain at 94 GHz with four stages from 0.91·2.98 mm^2 [3]. Cascodes with a gate length of 0.15 µm and two fingers of totally 100 µm width are used here for both stages to deliver high gain. Fig. 1 shows the layout of a cascode. The accurate modeling of cascodes as two transistors in one housing has been described earlier [4]. Input and output matching networks to 50 Ω with DC blocking capacitors use reactive matching. Open stubs which can be used for the input matching were replaced by MIM capacitors to reduce the chip area. The gate bias is supplied via quarter wavelength stubs whereas the drain bias networks are part of the interstage or output matching networks, respectively. The circuit topology of the amplifiers is similar to MMICs we reported previously using single HEMTs [5,6]. A photograph of chip is given in figure 2.

MMIC performance

Full two port corrected S-parameter measurements were carried out in the frequency range from 0.5 to 115 GHz on wafer to characterize the 2-stage 60 to 80 GHz LNAs. Figures 3 and 4 show the four S-parameters in the frequency range of interest. The LNAs were stable over the entire measurement bandwidth. The maximum gain varied between 28 and 32 dB for LNAs from three different wafers. The output matching was expected to be better, but the realized transistors had a higher output conductance due to shorter gate length than in the model. The predicted noise figure is less than 5 dB.

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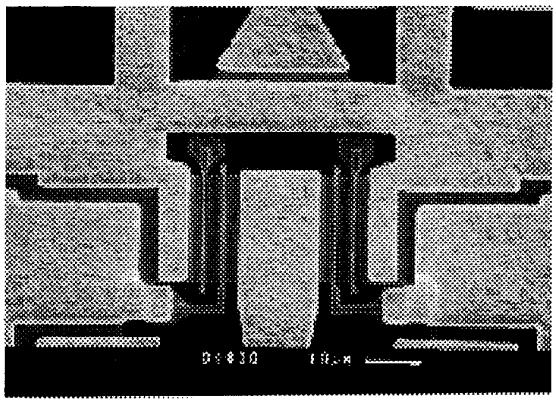

Fig. 1 A cascode pair of transistors in an MMIC.

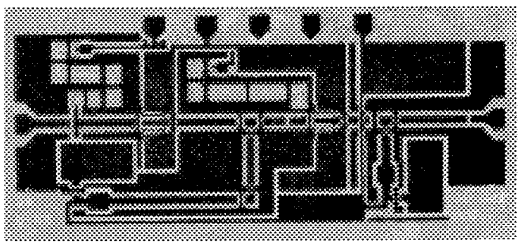

Fig. 2 2-stage 60-80 GHz LNA. The chip size is $0.59 \cdot 1.4\ mm^2$.

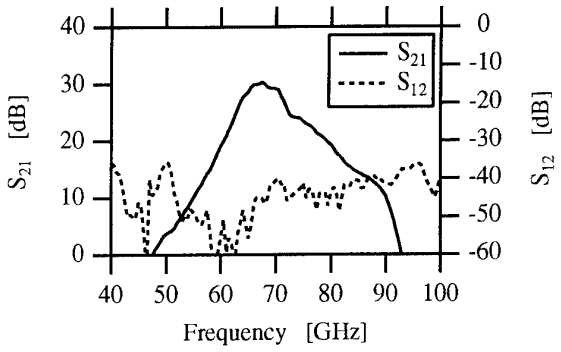

Fig. 3 Measured gain and reverse isolation for the 2-stage LNA.

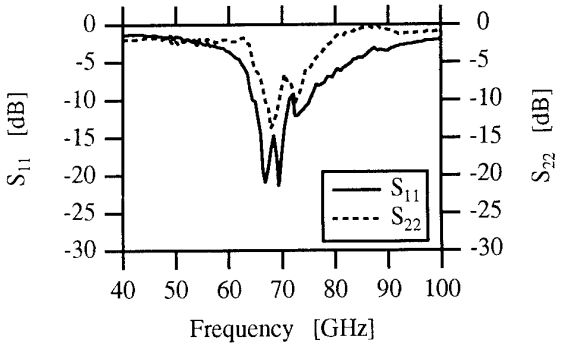

Fig. 4 Measured input and output matching for the 2-stage LNA.

Monolithic demodulator for high-sensitivity 5 Gbit/s CPFSK receiver using a distributed mixing principle

P. Karlsen, F. Ebskamp*, A. K. Petersen** and P. Danielsen

Center for Broadband Telecommunications
Electromagnetics Institute
Technical University of Denmark

*DSC Communications, Brøndby, **University of California, Santa Barbara, CA

Abstract: A distributed GaAs MMIC MESFET mixer is designed and applied in an integrated CPFSK demodulator, with an input IF bandwidth of 7GHz and a baseband bandwidth of 4GHz, yielding a receiver sensitivity of -39dBm at 5Gbit/s.

Introduction: Concerning receiver sensitivity and effective utilisation of the fiber bandwidth, the coherent optical system is competitive to the traditional intensity modulated direct detection (IM/DD) system. The coherent CPFSK (Continuous Phase Frequency Shift Keying) scheme has become common, because it can be achieved by direct modulation of the transmitter laser, and because the demodulation can be performed by a simple delay-and-multiply circuit in a heterodyne receiver. The compact CPFSK spectrum makes it possible to multiplex hundreds of high bit rate channels in the same fiber [1], which requires a large number of compact, low-cost and low-power receivers. These demands can be fulfilled by a high degree of monolithic integration in the IF stage of the receiver [2-5].

The required IF bandwidth of the coherent receiver is approximately two times the bit rate, which puts severe demands on the mixer input bandwidth. In this paper, we present a GaAs MMIC mixer designed to operate as the key element in an integrated CPFSK demodulator for a bit rate of 5Gbit/s. The mixer is realised in the low-cost F20 process from GEC Marconi, a 0.5μm MESFET process with an f_T of 20GHz. We have obtained an input bandwidth of 10GHz and an output bandwidth of 5GHz. System experiments are carried out employing the demodulator in an existing 5Gbit/s system operating at an IF just below 11GHz.

MMIC mixer: For obtaining the required input bandwidth, a distributed mixing principle, applying two Gilbert-cell multipliers, has been used [6]. The virtuel ground on every source terminal of the FETs in the cell couses an input impedance dominated by the gate-source capacitance of the transistors. These shunt capacitances are included in an artificial transmission line, making high impedance lines interconnecting the cells form the series inductance of the transmission line. Fig. 1 shows the schematic of the distributed part of the mixer with two Gilbert-cells, four gate-lines and two drain-lines. The gate-line impedances are 75Ω, while the drain-line impedances are designed to 50Ω to ensure a satisfactory output match. To avoid a low frequency cut-off in the baseband, the mixer output is direct coupled.

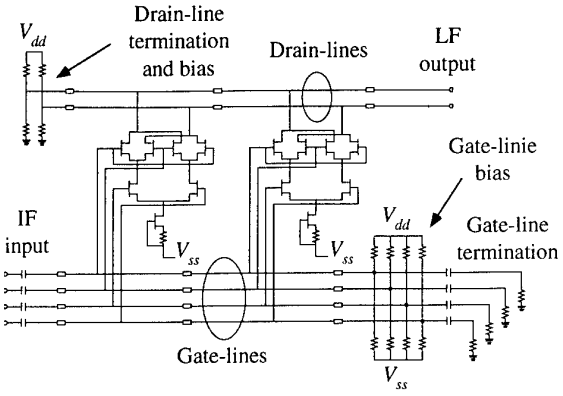

Fig. 1 *Gilbert-cell used in a distributed solution*

The double balanced input signals for the Gilbert-cell were generated by two on chip baluns consisting of an inverting common source amplifier and a non-inverting common gate amplifier (Fig. 2).

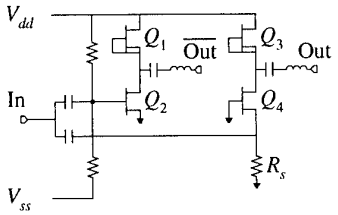

Fig. 2 *Input balun*

The input impedance of the balun is approximately R_s in parallel with $1/g_m$ of the common gate transistor and can thereby be matched to 50Ω. Since R_s also determines the gate-source voltage of Q_4, there is only a limited freedom in the choice of FET sizes. During simulations the balun phase error was less than 18°, while the gain difference of the inverting and non-inverting stage was below 1 dB in the frequency range 5-15GHz.

The chip layout was complicated by the distributed design, where 4 gate-lines and 2 drain-lines had to pass through the Gilbert-cell. It was carefully considered how to place the transistors, so that this was possible at all with only two metal layers. The resultant solution is seen on the chip photo in Fig. 3. The chip area occupied by the mixer is 4.5 mm^2.

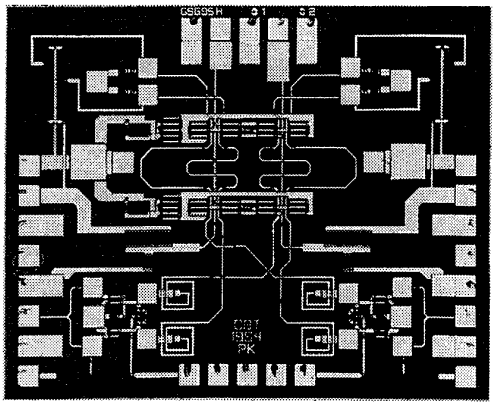

Fig. 3 *Chip photo of distributed MMIC mixer*

The mixer conversion characteristics were measured on-chip [7] showing that, a satisfactory input and output bandwidth were obtained at the expence of a low conversion gain of about -49dB.

Integrated demodulator: The mixer was mounted on a 1 × 1.5 inch alumina substrate, shown in Fig. 4, together with a three-section Wilkinson power divider and a 160ps delay line. The mixer is followed by a commercial HBT GaAs MMIC baseband amplifier with a 12dB gain to compensate for a low output voltage swing.

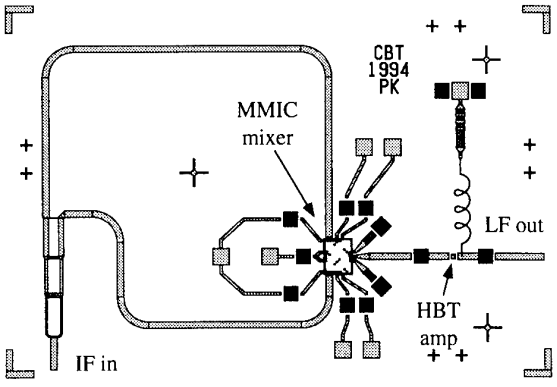

Fig 4 *Integrated 5 Gbit/s CPFSK demodulator*

By applying a swept synthesiser at the demodulator input, the discriminator curve was measured as the DC-voltage at the mixer output, and a zero crossing of about 10.6GHz was observed [7].

System experiments: The integrated demodulator was applied in a 5Gbit/s CPFSK system set-up, where 1549nm wavelength MQW-DFB lasers were used as transmitter and local oscillator. The transmitter laser was directly modulated at 5Gbit/s with a modulation index of 0.72. The IF bandwidth was 7GHz, and the demodulator was operating at an IF of 10.8GHz. Further details are given in [7]. A receiver sensitivity of -39.0dBm corresponding to 194 photoelectrons per bit was obtained at a bit error rate of 10^{-9}. This is less than 8dB from the theoretical shot noise limit.

Conclusions: By choosing a distributed principle in the design of a GaAs MMIC mixer for a 5Gbit/s CPFSK demodulator, it has been possible to comply with the stringent IF bandwidth demands even though, a low-cost MESFET process has been used. An input bandwidth of 10 GHz and an output bandwidth of 5 GHz are obtained for the mixer, and the applicability of the integrated demodulator is demonstrated in a 5Gbit/s system experiment by a high receiver sensitivity of -39dBm.

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High performance circuits using AlInAs/GaInAs/InP HEMTs

W. Patrick, M. Schefer, B-U.H. Klepser, H.C. Duran and Hp. Meier.

Laboratory for Electromagnetic Fields and Microwave Electronics
Swiss Federal Institute of Technology, Gloriastrasse 35, CH-8092 Zürich
Tel. 01 632 5978, Fax 01 632 1198, e-mail patrick@ifh.ee.ethz.ch

At recent WOCSDICE workshops, we have presented selected topics from our process development work; the basic process technologies and more recently the fabrication and modelling of high performance InP-HEMTs. In this presentation we will show how these technologies are now being applied to the fabrication of demonstration type integrated circuits.

Our processing strategy is as follows: The HEMT layers are grown externally by a commercial supplier but all other process steps are carried out in our laboratory. A reliable 'mix and match' lithography has been established where non-critical layers are defined using contact photolithography leaving only the 0.2 μm gates to be defined by electron-beam lithography. The latter is carried out using a modified SEM system which has been fitted with the ELPHY system (Raith) and a high precision laser interferometer stage. For thin film resistors and insulation layers, 'make-do' solutions have been found, namely evaporated Ti for the resistors and SiO for the insulator. For mm-wave circuits, an electroplating technology for patterning low resistivity interconnections has been developed. Fig. 1 is an SEM micrograph of one of our standard HEMTs with an 0.2 μm T-gate. Fig. 2 shows a multi-finger HEMT with an airbridge connecting source contacts.

Using the above technologies, several circuits have been fabricated. One important application for InP HEMT devices is the mm-wave amplifier. As a first step, several single stage amplifiers using transmission line or shorted stub matching networks (all using coplanar waveguide technology) were designed and fabricated. The best on-wafer performance was obtained for an amplifier with stepped impedance matching (Fig. 3). A bandwidth of 20 GHz with a centre frequency of 60 GHz was obtained. For a single stage amplifier, the gain was extremely high; 9.1dB at 64 GHz and 4 dB at 75 GHz. These single stage amplifier circuits will be used as the basis for designing the next generation of amplifier circuits with 2 or more stages.

For high bit-rate photoreceiver circuits (> 10 Gbit/s), two types of amplifier circuit have been designed: a 2-stage common source amplifier with feedback (transimpedance amplifier) and a high input impedance 2-stage common source amplifier. Both circuits yielded a bandwidth of 15 GHz with transimpedance values of around 47 dBΩ (Fig. 4). With this performance it should be possible to fabricate a photoreceiver for 20 Gbit/s when the circuit is integrated with, for example, a pin-diode.

These two examples show that high performance can be obtained using straightforward processing technologies, which is an attractive feature of InP HEMT technology. The circuits are not fully optimised in terms of reliability (Ti resistors, not passivated), but for the purposes of demonstrating circuit performance this is not yet a major issue.

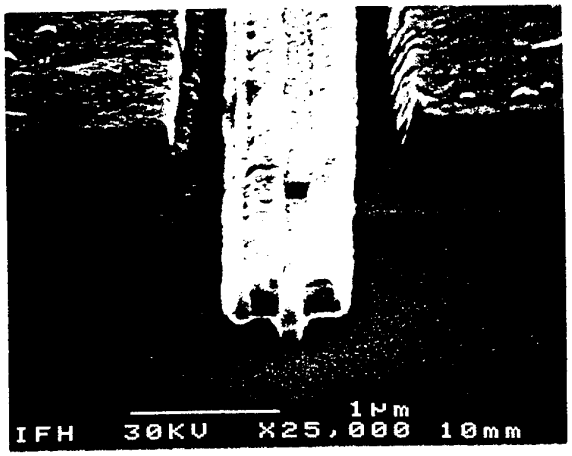


Fig. 1: SEM micrograph of an 0.2 μm HEMT device

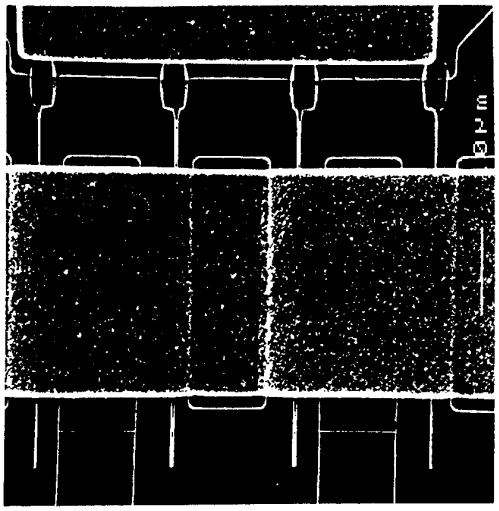
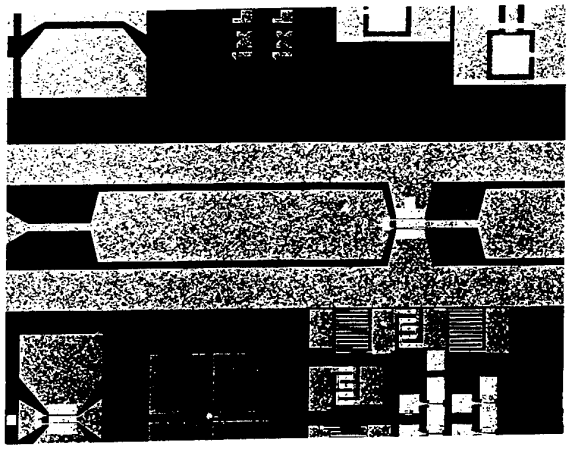


Fig. 2: SEM micrograph showing a 4 gate finger HEMT



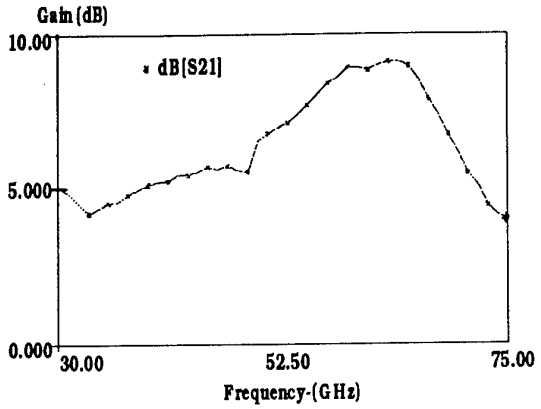
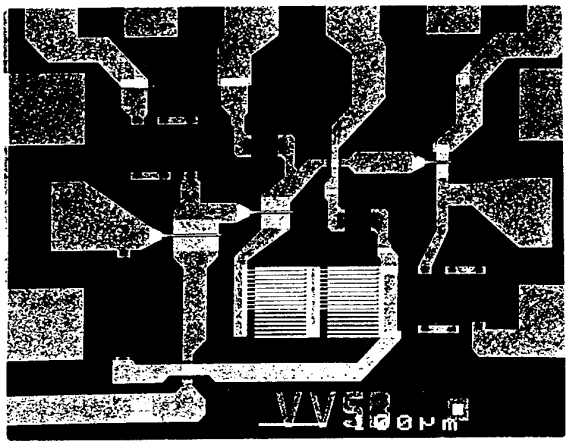


Fig. 3: SEM micrograph of a stepped impedance, single stage mm-wave amplifier and measured gain of this circuit



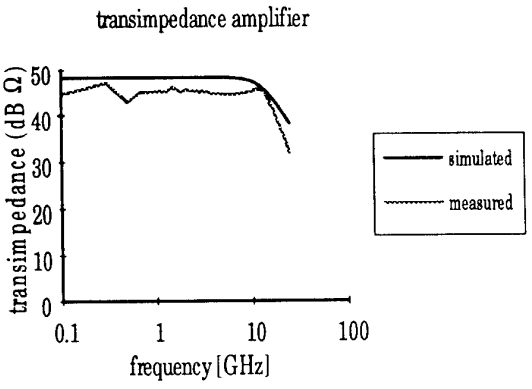


Fig. 4: SEM micrograph of a transimpedance amplifier and measured transimpedance as a function of frequency.

Transconductance dispersion in LT GaAs MISFET's.

B. Boudart, E. Delos, F. Ducroquet, H. Gérard, D. Théron,
M. Lipka,* B. Splingart* and E. Kohn*

Institut d'Electronique et de Microélectronique du Nord, U.M.R. - C.N.R.S. 9929
Département Hyperfréquences et Semiconducteurs, Avenue Poincaré, B.P. 69
59652 VILLENEUVE D'ASCQ CEDEX - FRANCE

* Universität Ulm, Department of Electron Devices and Circuits
Albert Einstein Allee 45
86069 ULM - GERMANY

ABSTRACT.

LT GaAs MISFET's present higher breakdown voltages than similar GaAs MESFET's. They have shown high I×V products [1] overriding the limitation given by the lateral spreading model [2]. They also present a transconductance dispersion in the MHz range [3]. The transconductance may be reduced by a factor of 2 or even more at microwave frequency.

The basic structure is shown in figure 1. In this structure the LT GaAs passivates the gate drain region in such a way that the breakdown voltage is increased. High frequency measurements show that the RF transconductance is reduced compared to the dc value. This behaviour is attributed to the presence of the LT GaAs/AlAs insulator. This phenomenon is associated with a reduction of the S_{21} parameter in the 50-500 MHz range (figure 2). We have studied this dispersion by pulse I-V characteristics. We see a reduction in the transconductance at short pulse durations (figure 3). Small and large signal measurements are presented.

We have also performed power measurements at 100, 500 and 850 MHz in order to study the RF behaviour of the device. Different resistive load lines have been put at the output of the device. The results are compared to the values calculated from the dc characteristics. A discussion will follow.

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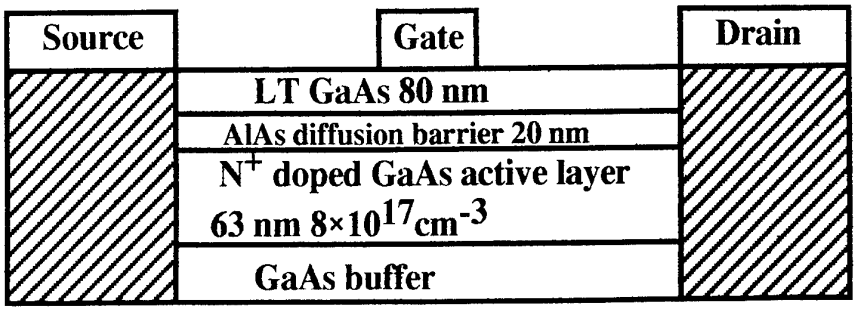

Fig. 1 : LT GaAs MISFET structure.

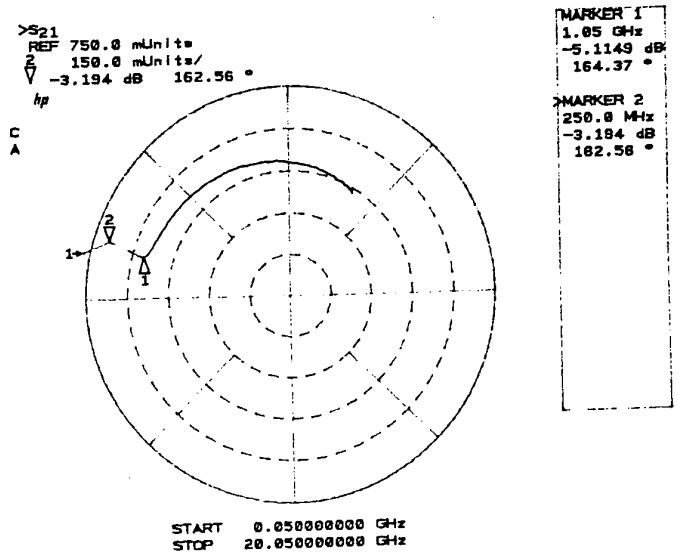

Fig. 2 : S_{21} parameter of the LT GaAs MISFET (V_{gs} = 0 V, V_{ds} = 3 V. S_{21} is decreasing between 50 and 1000 MHz.

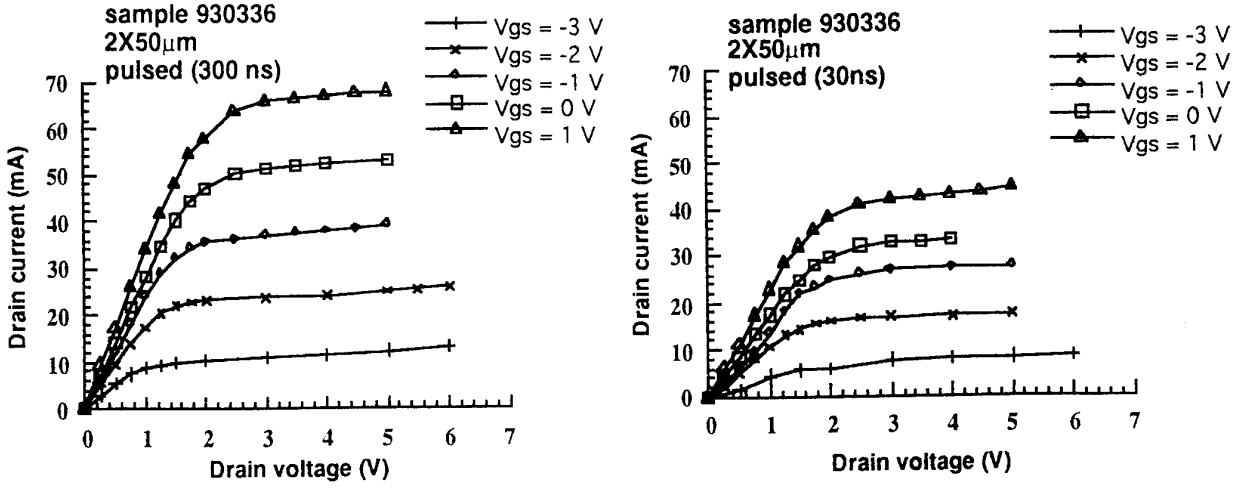

Fig. 3 : Pulsed characteristics for 300 and 30 ns pulse duration.

Delay Times in Lattice Matched InGaAs/InP HEMT's with Gatelengths between 80 and 250 nm.

J. Finders, Y. Baeyens*, D. Schreurs*, M. Van Hove, W. De Raedt, B. Nauwelaers*, M. Van Rossum

Interuniversity Microelectronics Center (IMEC), Kapeldreef 75, B-3001 Leuven
*K.U. Leuven, Div. ESAT-TELEMIC, K. Mercierlaan 94, B-3001 Leuven
Belgium

There is an increasing interest in both lattice matched (LM) and pseudomorphic (PM) InGaAs/InP HEMT's for high frequency applications. Their unity current gain cut off frequency f_T, which is an important figure of merit for high frequency applications increases for small gatelengths since the intrinsic delay of the carriers diminishes. Delay time measurements for 0.4 to 5 μm-gatelength HEMT's were reported by Enoki et Al.[1]. For smaller gatelengths the transit time of the electrons is decreased to the same order of magnitude as the extrinsic delays, such as the charging time of the bond pad capacitances. Thus, a further increase of the f_T can only be obtained by decreasing both the intrinsic (e.g. the gatelength) and the extrinsic delays. In this paper we extract the intrinsic and parasitic delay times for lattice matched InGaAs/InP HEMT's with gatelengths below 0.4 μm.

The layer structure for the fabrication of the LM InGaAs/InP HEMT's consists of a doped 7 nm InGaAs contact layer, a 20 nm undoped InAlAs layer, a δ-doping of 5×10^{12} at/cm^2, a 6 nm InAlAs spacing layer and a 20 nm $In_{0.53}Ga_{0.47}As$ channel which is separated from the InP substrate by a 250 nm $Al_{0.48}In_{0.52}As$ layer. Low resistance ohmic contacts (<0.1Ωmm) were created using Ni/AuGe/Ni/Au metallisation. The T-Gates were aligned in a bilayer resist (PMMA/Copolymer) using a JEOL XSM 840 SEM controlled by an ELPHY 2 system. Finally, after adjusting the threshold voltage (V_t) by wet recess etching in a phosphoric/hydrogen peroxide/water solution, Pt/Ti/Pt/Au gate metallisation was performed.

After device fabrication DC-measurements were carried out. Fig. 1 shows the I_{ds}-V_{gs} characteristics and the calculated DC transconductance g_m of a HEMT with 80 nm gatelength. A very low gate leakage current of about 1 μA at a gate voltage of -1 V was observed for all devices. They all pinch off very well at a threshold voltage of about -0.9 V which indicates a shallow recess etching. We observed no significant change of the g_m with decreasing gatelength: for all devices the g_m was 800 ± 20 mS/mm. It is expected that this relatively low g_m caused by the large channel-to-gate separation will give rise to substantial extrinsic delays in HF measurements. In a small signal model that takes into account the charging times associated with the gate pad capacitance (C_{pad}), the gate-drain capacitance (C_{gd}) and the transit time through the depleted drain region (drain delay, t_{drain}) the total delay time t_T is given by[2]:

$$t_T = t_{pad} + t_{par} + t_i + t_{RC} + t_{drain} = \frac{1}{2\pi \cdot f_{T_{extrinsic}}}$$

where t_i is the intrinsic transit time of the electrons, which directly scales with the gatelength L_g and the saturation velocity v_{sat}, and t_{RC} is the channel charging time. The intrinsic and extrinsic delay times were extracted from S-parameter measurements between 45 MHz and 26 GHz using the method of Moll et Al.[3]. Fig. 2 shows the total extrinsic delay time (t_T), the corrected extrinsic delay time (t_T with subtraction of t_{pad} and t_{par}) and the intrinsic delay time (t_i) as a function of the gatelength. The capacitance of the 70*75 μm^2 pad is about 15 fF and gives rise to a charging delay time of 0.2 ps for our devices of 100 μm width. The charging of the gate-drain capacitance C_{gd} through the source and drain resistance R_S and R_d leads to an additional parasitic delay (t_{par}) in the order of 0.1 ps. For the smallest gatelength the total delay time of 0.99 ps implements a f_T of 162 GHz, whereas in the absence of the pad and the parasitic delay a f_T of 229 GHz would have been achieved. To overcome this limitation of the f_T, a higher g_m would be desirable to reduce the pad

capacitance charging time. This can be accomplished by a better control of the recess etching and/or by switching to PM InGaAs/InP HEMT's. For pseudomorphic InGaAs/InP HEMT's extrinsic g_m's of 1700 mS/mm have been reported[4]. The parasitic delay and the drain delay of both 0.1 ps can be diminished using a self aligned process in which the R_S and R_d are substantially reduced by decreasing the source-gate and gate-drain spacing [2].

SUMMARY AND OUTLOOK

We used delay time measurements as an important tool for the optimisation of InGaAs/AlInAs HEMT's. For the devices presented in this paper the extrinsic delays, such as the pad capacitance charging time, are of the same order as the electron transit time. Therefore a further reduction of the gatelength below 80 nm is not very effective in increasing the extrinsic current unity gain cut-off frequency, which is 162 GHz for the smallest device (80 nm gatelength). These devices may well serve in circuits for high frequency applications such as broadband distributed amplifiers for which frequencies above 100 GHz should be accessible.

ACKNOWLEDGEMENT

Part of this work was carried out within a community training project financed by the Commission of the European Communities (HCM).

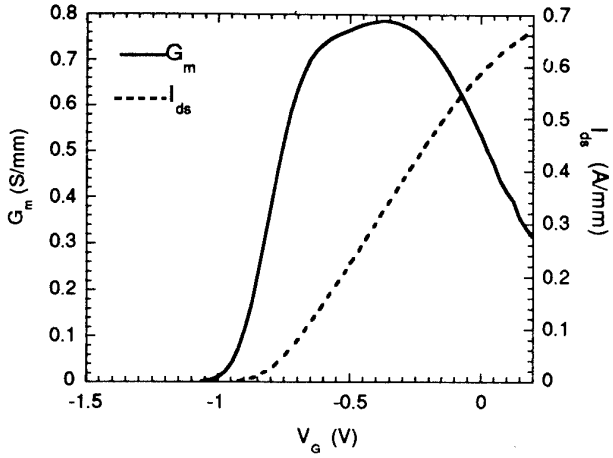

Fig. 1: I_{ds}-V_{gs} characteristics of a 0.080*100 μm^2 LM InGaAs/InP HEMT at V_D=1V (dashed line) and calculated extrinsic transconductance g_m (solid line).

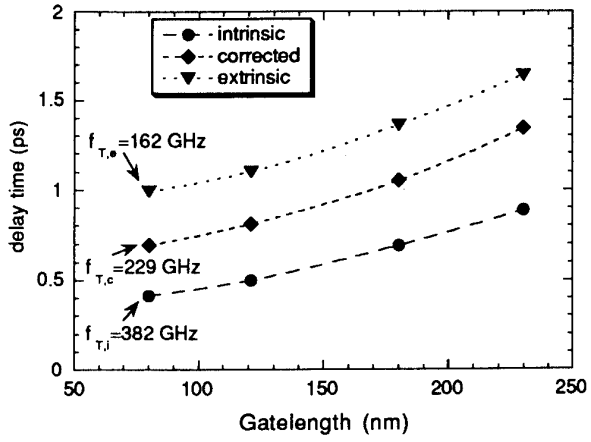

Fig. 2: Delay times as a function of the gatelength.

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SESSION 9

CHARACTERIZATION

On-Wafer Electro-Optic Testing of High-Speed Electronic Devices

M. K. Jackson
Dept. of Electrical Engineering, University of British Columbia
2356 Main Mall, Vancouver, B.C., V6T-1Z4, Canada
tel. (604)822–6348, fax (604)822–5949, email mikej@ee.ubc.ca

High-speed heterostructure devices have been developed which operate at extremely high frequencies. For example, resonant-tunneling devices have demonstrated oscillation at frequencies above 700 GHz. Three terminal devices such as modulation-doped field-effect transistors (MODFETs) have cutoff frequencies well above 300 GHz. These developments challenge our abilities to measure device operation. This talk will focus on electro-optic sampling, which is one of the most promising techniques for measurements of very-high-speed electronic devices.

Electro-optic sampling uses ultrafast optical pulses to probe voltages using the electro-optic effect, and exists in several forms depending on the probe geometry and source of electrical input to the device under test. The embodiment we are using is shown in Fig. 1: pulses from the mode-locked laser are divide by a beamsplitter; one pulse train excites a photoconductive switch, sending an electrical input to the device under test; the second passes through a variable delay, an electro-optic transducer and then goes to a polarization analyzer. Because pump and probe are derived from the same pulse train, this approach is jitter free. We use an external electro-optic transducer, which can be positioned at varying height above the electrodes.

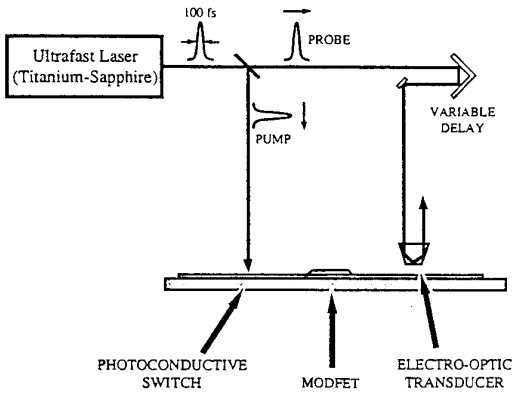

Fig. 1: Schematic of Experiment

The high dielectric constant of the $LiTaO_3$ probe can disturb signal propagation if placed too close to the coplanar electrodes. In Fig. 2 we show the measured risetime of a step-like input signal as a function of the separation between the probe tip and the coplanar electrodes. A significant increase in measured risetime can be seen as separation drops. We will discuss this behavior, and show data for the accompanying decrease in sensitivity.

Because electro-optic sampling probes the instantaneous voltage (or more precisely the field), it is incapable of distinguishing between incident and reflected signals. We will discuss a technique we have developed to separate overlapping signals, based on the difference in propagation directions. We make measurements at two closely-spaced locations. At the first location the input signal is seen, followed by the reflection. We then move closer to the device input, and make another mea-

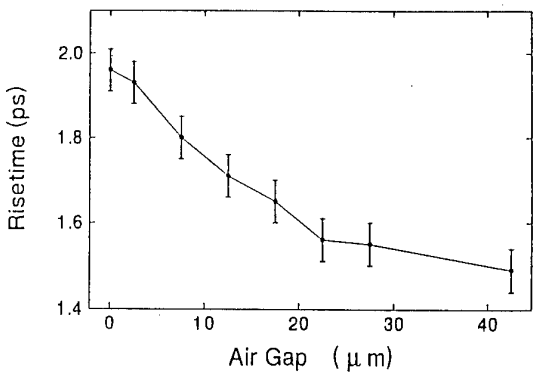

Fig. 2: Step function risetime as a function of sampling tip to electrode separation.

surement; the input signal is slightly delayed, and the reflection slightly advanced by the change in sampling position. If the two sampling locations are close together, the reflected and incident signals can be recovered from the two measurements. Data demonstrating this approach are shown in Fig. 3.

Finally we will discuss our recent measurements of MODFETs. A significant challenge with active devices is incorporation into a test fixture, which is usually a coplanar transmission line environment with transmission lines connected to input and output ports. We use the common-source configuration. The layout of the test fixture is sketched in Fig. 4; the structure of the photoconductive switches on input and output sides allows us to set the operating point of the transistor. The significant progress we have made is to monolithically-integrate the MODFET with the test fixture, *on-wafer*. This provides excellent control over access parasitics, and is far superior to the wire bonding used in previous work. A photograph of one of the integrated MODFETs is shown in Fig. 5. In Fig. 6 we show the response of an InAlAs/InGaAs device lattice-matched to InP, with a 0.35μm T-shaped gate. The top panel shows the input signal, which is step-like; the gate reflection starts at approximately 15ps. The lower panel shows the drain output signal, starting from the dc operating point of 0.8V. The two curves in Fig. 6 share the same time axis, and from this the absolute delay of the MODFET can be measured. We will present data for different biases and electrode configurations; drain switching times as short as 4.2 ps are seen, and the MODFET delay is measured to be as short as 3.2 ps. To our knowledge these are the fastest direct measurements of transistor switching reported.

Acknowledgements: The author would like to acknowledge the contributions of A. Zeng, S. A. Shah, W. Wong, M. Van Hove, and W. De Raedt to this work.

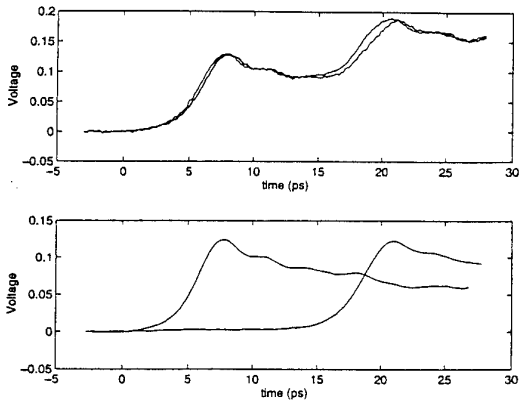

Fig. 3: Measured voltage at input to a coplanar stripline open circuit (upper). Recovered incident and reflected signals (lower).

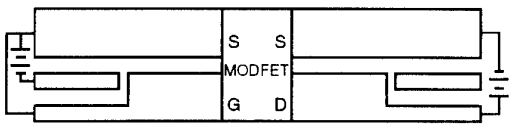

Fig. 4: MODFET test fixture schematic.

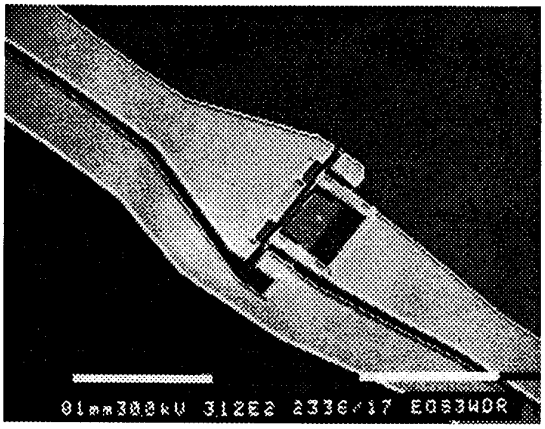

Fig. 5: Integrated MODFET/test fixture.

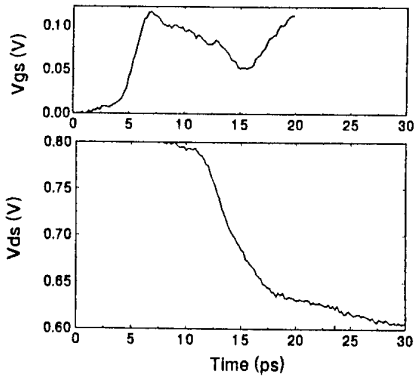

Fig. 6: Typical MODFET step response.

Fourier Transform Photoluminescence Excitation Spectroscopy of InGaAs/InP Quantum Wells with various strain and well width

J. Dalfors[a], T. Lundström[a], P.O. Holtz[a], B. Monemar[a], J. Wallin[b], and G. Landgren[b]

[a] Department of Physics and Measurement Technology, Linköping University, S-581 83 Linköping, Sweden

[b] Department of Electronics, Electrum 229, The Royal Institute of Technology, S-164 40 Kista, Sweden

ABSTRACT

Eversince the development of high precision growth techniques made it possible to routinely fabricate thin epitaxial layered structures such as quantum wells (QW:s), there has been a great interest in these structures from both a theoretical and an experimental point of view. The InGaAs/InP system is important for optical fiber communication, LED:s and QW lasers. In order to achieve optimal performance of these applications, it is important to know the electronic structure of the confined particle states in the QW. Two important parameters for the electronic stucture is the width of the well and the lattice mismatch between the well and the barriers i.e. the strain. For the fabrication of QW lasers it is of great importance to reduce the Auger processes which compete with and reduce the radiative recombination processes. Most high performance QW lasers are based on strained layer QW:s since the rate of Auger recombinations is reduced. This is believed to be due to the larger splitting between the valence sub-bands in the strained QW:s which reduces the probability for allowed Auger transitions but the details of the physical mechanism behind the improvement is not known. Therefore it is of great technological importance to improve the level of knowledge on the optical properties of strained InGaAs/InP QW:s.

To get information on the electronic structure at low temperature, photoluminescence excitation (PLE) spectroscopy is a very powerful technique. The usual way to get an excitation spectrum is to continuously change the energy of the exciting photons. When the excitation energy is resonant with the energy of an excited state, the photons are absorbed and electron-hole pairs are created, which very fast relax to the ground state where they recombine and thus give rise to an increase in the detected luminescence intensity.

For the energy range of the InGaAs/InP system there have been no tunable laser sources available up to now. Instead a scanning monochromator after a broadband light source has been used to excite the sample, as done by e.g Gershoni et al. Skolnick et al measured QW:s with different well width by conventional absorption.

In this work, a new technique for optical spectroscopy, Fourier transform photoluminescence excitation (FTPLE) spectroscopy together with Fourier transform photoluminescence (FTPL) spectroscopy has been employed to optically characterize different InGaAs/InP QW samples. It is a high precision technique that offers several advantages over dispersive spectroscopy in the required energy range. Here we present the first systematic investigation of the electronic structure of InGaAs/InP single QW:s dependence on strain and well width using this new technique.

The $In_XGa_{1-X}As$/InP QW structures were grown by metal organic vapor phase epitaxy (MOVPE) on n-type InP substrates. On top of the substrate a 2000 Å thick InP buffer layer was grown, followed by the InGaAs single QW and a 500 Å thick InP cap layer. Two different series of samples were used. In the first series, three different well widths, 100 Å, 150 Å and 250 Å, with constant composition were used. In the second series, the QW width was kept constant, L_Z=150Å, while the strain was varied from tensional to compressional.

The confinement effect is clearly seen in the FTPL spectra for different well width.The FTPL measurements also reveal a strong shift of the PL peak with strain. With the FTPLE technique we have detected and identified allowed ($\Delta n=0$) excitonic transitions from higher excited states up to n=3 related to both the heavy hole (hh) and the light hole (lh) subbands. Also the forbidden n=3 electron to n=1 hh transition is observed. The FTPLE spectrum of the tensionally strained structure has a general stucture that differs from the others since the n=1 hh and lh states are interchanged. The energy of the identified transitions are compared with calculations based on an effective mass model and bulk deformation potential theory.

Photoconduction and Internal Photoemission in PHEMTs

Fritz Schuermeyer, Charles Cerny, Ross Dettmer, J.P. Loehr, and R.E.Sherriff

Wright Laboratory, Wright Patterson AFB, OH 45433, (513) 255 8649

Photoelectric techniques such as photoreflectance and photoluminescence are routinely used in the evaluation of heterostructure materials. These techniques give information on the energy configuration. These techniques are not used on wafers containing fully fabricated HEMTs with submicron gate length since the top metal interferes with such measurements and also a relatively large area is tested.

We extended photoelectric evaluation to fully fabricated PHEMTs with submicron gatelength by illuminating the devices from the backside and by evaluating photocurrents rather than reflected light. We perform non-destructive on-wafer measurements. This evaluation technique is feasible since the bandgap of the substrate is larger than that of the channel and hence light can reach the active transistor area with minimal absorption if the photon energy is less than the substrate bandgap. The spectral dependance of the photocurrent allows the evaluation of the photon absorption in the channel and gives information on the energies of the hole and electron sublevels. The resulting energies are different from those measured on the heterostructure material since the gate metal changes the potential in the quantum well. The configuration of the well is further modified by the applied electric potentials.

The incident light generates electron-hole pairs in the channel. These photogenerated charges can be observed as photocurrents both at the drain and gate electrodes. Applying a potential between the drain and source electrodes allows the splitting of the charges with electrons flowing to the positively biased drain and holes flowing to the source. This photocurrent is due to the photoconductance within the quantum well. One observes an amplification of the electron current due to the different electron and hole mobilities. If the device is biased close to pinch-off, further amplification is observed. This strong amplification can be explained as follows: Near pinch-off the energy configuration along the channel from source to drain resembles that of a lateral junction bipolar transistor where the area beneath the gate corresponds to the base. This device is similar to a photo transistor where the photogenerated charge in the base is amplified.

The photogenerated holes and electrons will not reach the gate if they are perfectly confined to their respective wells. We observe photogatecurrents, indicating less than perfect confinement. Specifically we observe holes emitted from the channel to the gate. Amplification of this current component is neither observed nor expected. Transistors fabricated at different facilities show large differences in their photoemission characteristics.

The new photoelectric analysis technique for PHEMTs, described in this paper, provides for better understanding of the device physics by giving information on the location of the electron and hole sublevels and their dependance on applied bias conditions, by allowing evaluation of charge confinement in the channel, and by providing a measure of the quality of the source to channel junction.

CHARACTERIZATION OF p-TYPE MODULATION -DOPED SiGe HETEROSTRUCTURES BY OPTICAL SPECTROSCOPIES.

I. A. Buyanova, W. M. Chen, A. Henry, W. X. Ni, G. V. Hansson, and B. Monemar

Department of Physics and Measurement Technology, Linköping University, S-58183 Linköping, Sweden

During the last few years the SiGe/Si heterostructures have gained an increasing interest driven by the desire for new devices (such as infrared detectors with tunable spectral characteristics and high speed transistors), and for a possible integration of devices utilizing the low dimensional phenomena in SiGe/Si quantum wells with structures based on the well developed Si technology. One of the common ideas of such devices is to utilize the transport and optical properties of a two dimensional hole gas (2DHG) formed in the SiGe/Si quantum structures. In order to bring the material quality up to the high level needed for many devices, the basic mechanisms behind the observed physical properties of this material system must be understood. Here the physical processes of carrier recombination, which determine carrier lifetimes in the devices, are of fundamental importance.

In this work we demonstrate general applications of optical techniques, such as photoluminescence (PL) spectroscopy and optically detected cyclotron resonance (ODCR), as convenient and contactless tools to evaluate the quality of the materials and device structures and to characterize the recombination processes in modulation doped SiGe/Si heterostructures. These optical spectroscopies are known to be very sensitive and selective, and have in the past been shown to be highly successful in characterizing other semiconductor thin films and heterostructures. Modulation boron doped strained $Si/Si_{1-x}Ge_x/Si$ quantum wells (QWs) and Si epilayers, grown in our laboratories by MBE technique, are studied.

It is shown that the band bending and band filling of the SiGe QWs caused by the charge transfer of holes from the doped Si barriers manifest themselves as an appearance of a broad asymmetric PL band with a characteristic sharp high energy cut-off corresponding to the Fermi edge of the 2DHG. The filling of SiGe QWs was changed either by varying the structure

parameters such as the distance between the QWs and doping layer, the doping concentration, or by varying experimental conditions such as photo-excitation intensity and bias across the structures. The shape of the PL band was shown to depend critically on the Fermi level position with respect to the next unoccupied hole subband. In particular, a pronounced enhancement of the recombination probability is detected for transitions involving the states at the Fermi energy when the Fermi level is approaching but is slightly below the next unoccupied hole subband.

In boron modulation-doped Si layers the recombination between the 2DHG confined in the doped regions and nearby electrons gives rise to two asymmetric PL bands near the Si band edge. The participation of the 2DHG in the recombination process is confirmed by varying the doping level and hydrogen passivation, where a quenching of these PL bands with decreasing doping concentrations below the degenerate limit was observed. It is shown that the PL observed is composed of two components with their relative intensities depending strongly on the excitation power and the temperature. The proposed recombination mechanisms include the recombination of the 2DHG with electrons trapped by residual donors (the low energy PL component) and with free electrons (the high energy PL component) localised in the vicinity of the doped regions by a photo-induced potential. A low concentration of residual donors is responsible for the observed saturation of the low-energy PL with increasing excitation intensity. It is suggested that the thermally-activated release of free electrons from this potential is probably responsible for the observed strong thermal quenching of the high energy PL component, as a consequence of increasing spatial separation between the 2DHG and free electrons.

The ODCR technique, capable of measuring the effective masses and carrier mobility by monitoring the changes of luminescence intensity due to the cyclotron resonant absorption of microwave fields in an applied magnetic field, was utilized to evaluate the quality of the structures. It is clearly shown that the presence of severe ion bombardement processes during the growth of the structures may cause lattice distortion and a reduced mobility, in particularly in modulation doped structures.

ELECTRON TRANSPORT THROUGH GaAlAs BARRIERS

J.C. Bourgoin

Groupe de Physique des Solides, Universités Paris 6 et 7, C.N.R.S./URA 17,
Tour 23, 2 place Jussieu, 75251 Paris Cedex 05, France

Electronic transport perpendicular to heterostructures and barriers must be mastered in many devices. In some of them, e.g. resonant tunnelling diodes, it must be controlled and in others, e.g. photodetectors, it must be avoided.

The study of the current-voltage characteristics through single non intentionally doped GaAlAs barriers imbedded in n^+ doped GaAs have been monitored as a function of temperature (50 – 300 K), barrier thickness (100 – 2000 Å) and the nature of the spacer layer, a non intentionally GaAs layer introduced between doped GaAs and the GaAlAs barrier.

Analysis of the data demonstrate that the mechanisms inducing the transport are not tunnelling at low temperature and thermo-ionic emission at high temperature. The two dominant mechanisms have been identified. They are related to the presence of defects and the role of these defects has been verified by introducing controllable amounts of defects by electron irradiation. The defects involved are donor defects; in unirradiated barrier the defect is the DX center related to the residual donor impurities.

This study allows to understand the role the spacer layers play in the adjustment of perpendicular current as well as the evolution of the current amplitude versus the barrier thickness.

Luminescence and Magnetotransport Studies of InP-based HEMT structures

W.E. Leitch, B. Henle, E. Kohn.

Department of Electron Devices, University of Ulm, D-89069 Ulm/Donau FRG

Introduction

A well-established method for reducing the surface roughness and vertical spread of impurities in HEMT structures has been the growth of a superlattice buffer between the substrate and the channel. This has been grown until now solely for its physical and chemical properties, and the study of its electrical transport properties has been neglected. A superlattice of InAlAs and InGaAs has velocity-field properties intermediate between the InGaAs and InP, and this suggests that a InAlAs/InGaAs superlattice sub-channel combined with an InGaAs sub-channel device will have improved velocity-field characteristics over InGaAs-alone structures.

For a systematic optimization of device parameters, one must have an understanding of the impact of different aspects of the technological process, from the heterostructure design, through the material analysis stages, to the device characterization. For accurate modelling of the proposed device, realistic materials parameters must be introduced, and the results of the modelling tested by experimental analysis. It has proved possible to reconcile these measurements in the GaAs-based material system [1,2], but progress in the InP-based system has been difficult, particularly with respect to reconciling the electrical measurements with the optical measurements. This is because the photoluminescence measurements give a static measurement of the carrier concentration in the channel of the structure at low temperature, whereas the Hall Effect measurements are affected by parallel conduction in the supply layer, and are measured at 77 K without the cap, and thus this is no longer a static measurement.

Measurements of the carrier concentration in InP-based HEMT structures by Shubnikow-de Haas and Hall Effect at 1.5 K have been reported, and these measurements show in general good agreeement with the modelling [3,4]. Luminescence studies of doped InGaAs / InP quantum well structures show enhancement of the luminescence at the Fermi edge [5], but no report until now has been made of the dependence of the luminescence on the quantum well carrier density at the doping levels and structures of interest for InP-based devices.

Material Growth

Two samples were grown by MBE on InP semiinsulating substrates, one with an InGaAs channel, and one with a InGaAs/InAlAs superlattice sub-channel and an InGaAs sub-channel. After a 5nm AlInAs-spacer, a Si δ-layer with $7x10^{12}cm^{-2}$ was deposited, then for contacts a 20nm AlInAs-layer and a doped 25 nm GaInAs-cap.

Characterization

Standard luminescence techniques were used to obtain spectra of the HEMT structures (see Figure (1)). The spectra show the expected step-like luminescence from the lowest sub-bands up to the Fermi-level. At the Fermi-level, there is a sharp cut-off, as above this energy there are a negligible number of carriers. This sharp cut-off is manifested by a change in gradient of the luminescence-energy plot at the Fermi energy. The calculated values for the carrier densities are indicated in Table (1). Hall measurements were performed at 77K, with the highly-doped cap layer removed, to provide values of the carrier density and mobility. For the two structures considered here, the Hall measurements of carrier density without cap at 77K are substantially higher than those derived from the photoluminescence spectra (see Table (1)). To confirm the value of the carrier density by the photoluminescence, Shubnikow-de Haas measurements were performed. The values derived show good agreement with those derived from the photoluminescence spectra. The measurements of the sub-band carrier density were used as fit parameters for the CBAND model [6] for a calculation of the total carrier distribution.

Table (1): Carrier Density measured by luminescence and SdH techniques

Sample	PL (sub-band 1)	PL (sub-band 2)	SdH (sub-band 1)	SdH (sub-band 2)	Hall (total)
1	2.1 e 12	5.3 e 11	2.06 e 12	5.66 e 11	7.57 e 12
2	2.1 e 12	5.8 e 11	2.02 e 12	5.66 e 11	5.32 e12

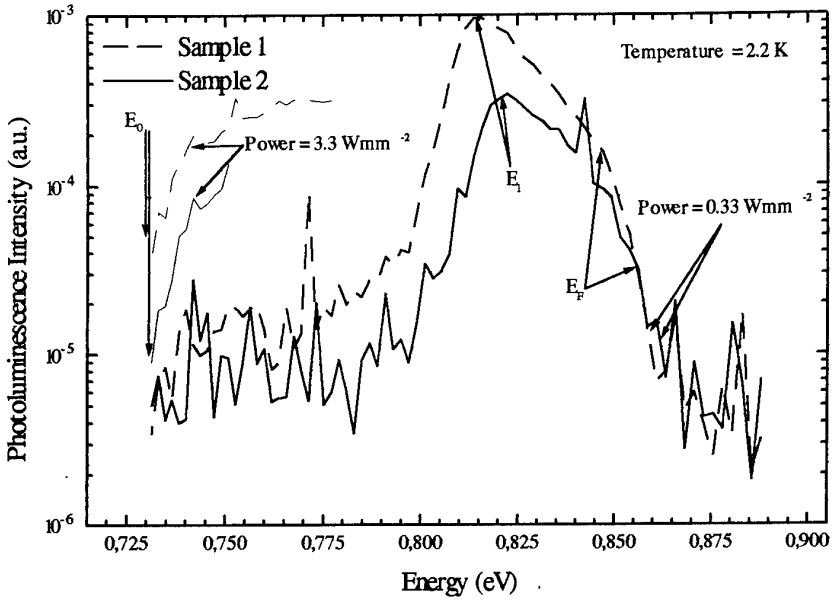

Figure (1): Photoluminescence Emission from HEMT structures

Figure (1) is composed from measurements at low and medium intensity to derive both E_0 and E_F.

E_F measured at low intensity to minimize thermal broadening, E_0 at medium intensity to extract the measurement from noise. E_0 position has negligible dependence on excitation density in this regime.

Results and Discussion

Good agreement is observed between the measurements of carrier density by luminescence and Shubnikow-de Haas techniques, whereas the Hall measurements without the cap at 77K give widely differing values. The Hall measurements cannot be explained by the parallel conduction in the supply layer, superlattice or buffer, as calculations by the CBAND model of the carrier concentration in these components of an ideal structure show parallel conduction to be negligible. The discrepancy between the Hall data and the model may be attributed to either incomplete removal of the cap layer or to the delta distribution modelling, and this will be discussed more fully in the workshop.

We would like to acknowledge the technical assistance of Mr. R. Rösch. The Shubnikow-de Haas measurements were performed by Dr. W. Limmer in the Semiconductor Physics Department, University of Ulm. This work was funded by an EU/HCM grant and the DFG.

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Ericsson Components AB
Communications Department
S-164 81 Stockholm, Sweden

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